# Table of Contents

1 Warranty ................................................................................................................................................. 4
2 Operating Specifications .......................................................................................................................... 5
  2.1 CSB726 Operating specifications ........................................................................................................ 5
3 Overview .................................................................................................................................................... 6
  3.1 Introduction ........................................................................................................................................ 6
  3.2 Block Diagram .................................................................................................................................. 6
4 On-Board Devices .................................................................................................................................... 8
  4.1 CSB726 Address Map .......................................................................................................................... 8
  4.1.1 Address Map Notes ......................................................................................................................... 8
  4.2 64Mbyte Spanion FLASH .................................................................................................................... 9
  4.3 128Mbyte Mobile SDRAM ................................................................................................................ 9
  4.4 512Mbyte 8-Bit NAND Flash ............................................................................................................ 9
  4.4.1 NAND Flash Notes .......................................................................................................................... 10
  4.5 SMSC LAN9211 Ethernet Controller .................................................................................................. 10
  4.5.1 LAN9211 Interface Notes ................................................................................................................ 11
  4.6 SM501 2D Graphics Coprocessor ...................................................................................................... 11
    4.6.1 SM501 Interface Notes ................................................................................................................... 11
    4.6.2 SM501 2D Graphics Controller .................................................................................................... 12
    4.6.3 SM501 LCD Panel Interface ......................................................................................................... 12
    4.6.4 SM501 LCD Notes ........................................................................................................................ 13
    4.6.5 SM501 Video Input Port ................................................................................................................. 13
    4.6.6 SM501 UARTs, SSP and I2C ......................................................................................................... 14
  4.7 SM501 Unavailable Ports ..................................................................................................................... 14
  4.8 DS1339 RTC ....................................................................................................................................... 14
    4.8.1 DS1339 RTC Interface Notes ....................................................................................................... 15
  4.9 LM3489 3.3V Regulator ...................................................................................................................... 15
    4.9.1 LM3489 3.3V Regulator Notes ...................................................................................................... 15
  4.10 SM501 Core Voltage Regulator ......................................................................................................... 16
    4.10.1 SM501 Core Regulator Notes ...................................................................................................... 16
  5 PXA270 On-Chip Peripherals .................................................................................................................. 17
    5.1 Overview .......................................................................................................................................... 17
    5.2 PXA270 to SODIMM Peripheral Mapping ...................................................................................... 17
    5.3 PXA270 Chip Selects ........................................................................................................................ 18
    5.4 PXA270 General Purpose I/O Assignments ..................................................................................... 18
    5.4.1 PXA270 GPIO Notes ...................................................................................................................... 22
    5.5 PXA270 Interrupt Pin Assignments .................................................................................................. 23
    5.6 PXA270 UARTS .................................................................................................................................. 23
      5.6.1 PXA270 UART Notes .................................................................................................................... 24
    5.7 PXA270 SSP/SPI Controllers ............................................................................................................. 24
      5.7.1 PXA270 SSP/SPI Interface Notes ............................................................................................... 25
    5.8 PXA270 I2C Interface ........................................................................................................................ 26
    5.9 PXA270 4-Bit SD/MMC Controller .................................................................................................... 26
    5.9.1 PXA270 SD/MMC Interface Notes ................................................................................................. 26
    5.10 PXA270 Compact Flash Interface .................................................................................................. 27
      5.10.1 PXA270 Compact Flash Interface Notes .................................................................................. 28
    5.11 PXA270 USB Host Controller ........................................................................................................ 28
      5.11.1 PXA270 USB Host Interface Notes .......................................................................................... 28
    5.12 PXA270 USB Device Controller .................................................................................................... 29
      5.12.1 PXA270 USB Device Interface Notes ...................................................................................... 29
    5.13 PXA270 AC97 Audio Codec Interface ............................................................................................ 29
      5.13.1 AC97 Audio Interface Notes .................................................................................................... 29
    5.14 Unavailable PXA270 Peripherals/Signals .................................................................................... 30
6 CSB726 Clocking ........................................................................................................................................ 31
    6.1 PXA270 Input Clocks ......................................................................................................................... 31
    6.2 PXA270 Output Clocks ........................................................................................................................ 31
    6.3 SM501 Clocks ..................................................................................................................................... 31
      4.129211 Clock .................................................................................................................................... 31
7 CSB726 Power Management .................................................................................................................... 32
    7.1 PXA270 PWR_EN (SODIMM *LOW_PWR) ................................................................................... 32
    7.2 PXA270 SYS_EN ............................................................................................................................... 32
    7.3 PXA270 Battery and VDD Fault ....................................................................................................... 32
    7.4 PXA270 Core Voltage ........................................................................................................................ 32
    7.5 SODIMM **PWR_DIS ....................................................................................................................... 32
8 SODIMM Software ................................................................................................................................. 33
    8.1 Overview .......................................................................................................................................... 33
9 SODIMM Format and Pinout ................................................................................................................... 34
    9.1 Overview .......................................................................................................................................... 34
    9.2 SODIMM Format ................................................................................................................................ 34
9.3 SODIMM Pinout................................................................. 34
10 Component Locations .......................................................... 42
10.1 Overview ........................................................................... 42
11 Document Revisions ............................................................ 43

List of Tables
Table 1 – CSB726 Operating Specifications......................................................... 5
Table 2 – CSB726 Address Map ....................................................................... 8
Table 3 – PXA270 to NAND Flash Connections ................................................. 10
Table 4 – PXA270 to LAN9211 Connections ..................................................... 11
Table 5 – SM501 to LCD Connections ................................................................. 13
Table 6 – SM501 Peripheral Multiplexing............................................................. 14
Table 7 – PXA270 to DS1339 Connections ........................................................ 15
Table 8 – PXA270 to SODIMM Peripheral Mapping ........................................ 18
Table 9 – PXA270 Chip Select Assignments ...................................................... 18
Table 10 – PXA270 GPIO Pin Assignments ....................................................... 22
Table 11 – PXA270 Interrupt Pin Assignments .................................................. 23
Table 12 – PXA270 UARTS to SODIMM Connections ........................................ 24
Table 13 – PXA270 SSP/SPI Controllers to SODIMM Connections ..................... 25
Table 14 – PXA270 I2C Controller to SODIMM Connections ............................... 26
Table 15 – PXA270 SD/MMC Controller to SODIMM Connections ................. 27
Table 16 – PXA270 to Compact Flash Connections ........................................... 28
Table 17 – PXA270 AC97 Controller to SODIMM Connections ......................... 29
Table 18 – PXA270 Unavailable Peripherals/Signals ......................................... 30
Table 19 – CSB726 SODIMM Expansion Connector Pinout ................................ 41
Table 20 – Document Revisions ...................................................................... 43

List of Figures
Figure 1 – CSB726 Block Diagram ................................................................. 7
Figure 2 – CSB726 Component Locations ....................................................... 42
1 WARRANTY

The enclosed product ("the Product"), a part of the Cogent Modular Architecture or Cogent Single Board series, is warranted by Cogent Computer Systems, Inc. ("Cogent") for a period of six months for reasonable development testing and use, all as further described and defined below. This warranty runs solely to the individual or entity purchasing the Product and is not transferable or assignable in any respect. This warranty is valid only for so long as the product is used intact as shipped from Cogent. Any attempt or effort to alter the Product, including but not limited to any attempt to solder, de-solder, unplug, replace, add or affix any part or component of or onto the Product, other than components specifically intended for the user to plug and unplug into appropriate sockets and/or connectors to facilitate user programming and development, all as specifically described and authorized in the Cogent Customer Product Users Manual, shall void this warranty in all respects. Coverage under this warranty requires that the Product be used and stored at all times in conditions with proper electrostatic protection necessary and appropriate for a complex electronic device. These conditions include proper temperature, humidity, radiation, atmosphere and voltage (standard commercial environment, 0°C to +70°C, <60%RH). Any Product that has been modified without the express, prior written consent of Cogent is not covered by this warranty. Cogent Single Board and Cogent Modular Architecture test and bus connectors are for use with Cogent adapters only. The use or connection of any test or bus connector, adapter or component with any device other than a Cogent connector or adapter shall void this warranty and the warranty of all other components, parts and modules connected to the rest of the system. Cogent shall not be responsible for any damage to the Product as a result of a customer's use or application of circuitry not developed or approved by Cogent for use on or in connection with the Product.

This warranty does not cover defects caused by electrical or temperature fluctuations or from stress resulting from or caused by abuse, misuse or misapplication of the Product. Any evidence of tampering with the serial number on the Product shall immediately void this warranty. This Product is not intended to be used on or embedded in or otherwise used in connection with any life sustaining or life saving product and this warranty is not applicable nor is Cogent liable in any respect if the Product is so used. Notwithstanding anything to the contrary herein, Cogent expressly disclaims any implied warranty of merchantability or implied warranty of fitness for a particular purpose in connection with the manufacture or use of the Product.
2 OPERATING SPECIFICATIONS

2.1 CSB726 OPERATING SPECIFICATIONS
The CSB726 conforms to the following specifications:

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimensions</td>
<td>68mm (2.63&quot;) x 50.8mm (2.00&quot;&quot;) x 8mm (.315&quot;)</td>
</tr>
<tr>
<td>Weight</td>
<td>~40g</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-20C to +100C</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>0C to +70C (Commercial Temp Version)</td>
</tr>
<tr>
<td>Humidity</td>
<td>0% to 95% RH, Non-Condensing</td>
</tr>
<tr>
<td>Input Voltage (VIN Pin)</td>
<td>+6V to +35V Maximum</td>
</tr>
<tr>
<td>VCC3 Output Voltage</td>
<td>+3.3V +/- 2% @ 2 Amp Output</td>
</tr>
<tr>
<td>Power Consumption (estimated)</td>
<td>750mw Typical, 1.5W Maximum</td>
</tr>
<tr>
<td></td>
<td>20mw Sleep to Ram</td>
</tr>
</tbody>
</table>

Table 1 – CSB726 Operating Specifications
3 OVERVIEW

3.1 INTRODUCTION
The CSB726 was designed and developed by Cogent Computer Systems, Inc. as a highly integrated Marvell® PXA270 System On a Module (SOM). The CSB726 provides a very small, powerful, flexible engine for embedded control systems of all kinds. The major features of the CSB726 are as follows:

- 520Mhz Marvell® PXA270 CPU with 32K I-Cache and 32K D-Cache
- 128Mbyte 32-Bit Wide Mobile SDRAM (<5mw Power Consumption in Sleep Mode)
- 64Mbyte 16-Bit Wide Spansion FLASH with Secure 256 Byte Sector and 128-Bit Unique ID
- 512MByte 8-Bit NAND Flash
- Silicon Motion SM501 LCD Controller with 2D Acceleration and 8Mbyte Frame Buffer, supports 18-Bit RGB Panels up to 1280 x 1024
- 8-Bit YUV4:2:2 or CCIR656 Video In via SM501 ZV Port, with YUV to RGB conversion
- Low Power LAN9211 10/100Mbit Ethernet Controller
- 12Mbit USB 1.1 Host and Device Ports
- DS1339 Real Time Clock with Battery Backup
- RS-232 Buffer for Debug Serial Port (PXA270 STDUART)
- 4 Additional TTL UARTS: one 8-Wire (PXA270 FFUART), one 4-wire (PXA270 BTUART) and two SM501 4-wire (shared with SM501 ZV Port)
- SSI/SPI (x3), AC97 and I2C buses for I/O Expansion such as Audio, A/D, D/A, etc.
- PXA270 SD/MMC Controller, 4-Bit, SDIO Compliant
- 26-Bit Address/16-Bit Data bus for Compact Flash or Generic Expansion
- Standard ARM JTAG Interface
- 10 Dedicated GPIO lines (most peripherals may also be assigned as GPIO)
- Programmable Core Regulator (0.9V to 1.5V) for Dynamic Voltage/Frequency Scaling
- Wide Input (6V to 35V), On Board 3.3V Regulator provides 2A to the User Board
- <750mw typical, 1,500mw maximum, <15mw sleep to RAM
- Compact SO-DIMM form factor, 2.63” (68mm) x 2.0” (50.4mm) x 0.315” (8mm) high
- Low EMI design with 0402 components and Fine-Line, Multi-Layer PCB construction
- Compatible with Cogent CSB702 Base Board

3.2 BLOCK DIAGRAM
Refer to the following figure for a block diagram of the CSB726 SOM.
CSB726 BLOCK DIAGRAM

520MHZ PXA270 XScale Core
- PWR_EN
- JTAG
- I2C
- S3P1
- S3P2
- S3P3
- FF UART
- BT UART
- STD UART
- AC97
- 4-BIT SD/MMC
- USB 1.1 HOST
- CHIP SELECTIONS AND CONTROL
- PCMCSA/COMPACT FLASH IF
- GPIO
- USB 1.1 HOST
- UART0
- UART1
- UART2
- ACPI
- SD/MMC
- USB DEVICE
- COMPACT FLASH CONTROL
- GPIO
- TOUCH & EXPANSION IRQ'S
- DEBUG SIO
- EXPANSION CHIP SELECT AND CONTROL
- 16-BIT DATA 25-BIT ADD.

SM501 2D GRAPHICS CONTROLLER
- 32-BIT DATA 25-BIT ADD.
- LCD DATA AND CONTROL
- ZV VIDEO INPUT PORT
- UART0
- S3P5/UART1
- 16-BIT DATA 8-BIT ADD. HOST I/F
- 8MBYTE FRAME BUFFER
- SPI
- LCD I/F
- SDRAM CONTROL
- CHIP SELECTS AND CONTROL
- 32-BIT DATA 25-BIT ADD.
- 16KBYTE RX/TX BUFFER
- PCMCIA/COMPACT FLASH I/F
- GPIO
- USB 1.1 HOST
- UART0
- UART1
- UART2
- ACPI
- SD/MMC
- USB DEVICE
- COMPACT FLASH CONTROL
- GPIO
- TOUCH & EXPANSION IRQ'S
- DEBUG SIO
- EXPANSION CHIP SELECT AND CONTROL
- 16-BIT DATA 25-BIT ADD.

LAN9211 10/100 CONTROLLER
- 10/100 TWISTED PAIR I/F
- STATUS LED'S
- 10/100 TWISTED PAIR I/F
- 256-BIT EEPROM
- PCMCIA/COMPACT FLASH I/F
- GPIO
- TOUCH & EXPANSION IRQ'S
- DEBUG SIO
- EXPANSION CHIP SELECT AND CONTROL
- 16-BIT DATA 25-BIT ADD.

JTAG
- SPI
- SPI1
- SPI2
- SPI3
- SPI (TOUCH)
- UART0
- UART1
- UART2
- ACPI
- SD/MMC
- USB DEVICE
- COMPACT FLASH CONTROL
- GPIO
- TOUCH & EXPANSION IRQ'S
- DEBUG SIO
- EXPANSION CHIP SELECT AND CONTROL
- 16-BIT DATA 25-BIT ADD.

128MBYTE, 32-BIT MOBILE SDRAM
- VCC3 MOUNTING HOLE & POWER TERMINAL 3.3V @ 2A OUT
- 3.3V @ 4A SWITCHING REGULATOR
- 3.3V @ 4A SWITCHING REGULATOR SMBUS I/F
- 3.3V @ 2A OUT
- 6V TO 35V IN
- 3.3V

64MBYTE 16-BIT SPANSION FLASH
- STATUS OUT
- 3.3V
- LED IS ON WHEN ERASING OR PROGRAMMING
- 512MBYTE, 8-BIT NAND FLASH
- VIN MOUNTING HOLE & POWER TERMINAL 6V TO 35V IN

DS1339 REAL TIME CLOCK
- 12/1/2007
- VCC3 MOUNTING HOLE & POWER TERMINAL 3.3V @ 2A OUT
- 3.3V

Figure 1 – CSB726 Block Diagram
4 ON-BOARD DEVICES

4.1 CSB726 ADDRESS MAP

The following table describes the Address Map of the CSB726. Refer to the PXA270 documentation for information regarding on-chip peripheral addressing.

<table>
<thead>
<tr>
<th>CPU Chip Select</th>
<th>Chip Select Width</th>
<th>Wait States</th>
<th>Address Start</th>
<th>Address End</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>*CS0</td>
<td>16</td>
<td>12</td>
<td>0x0000.0000</td>
<td>0x03FF.FFFF</td>
<td>S29GL512N</td>
</tr>
<tr>
<td>*CS1</td>
<td>N/A</td>
<td>N/A</td>
<td>0x4000.0000</td>
<td>0x07FF.FFFF</td>
<td>Used as GPIO15 (Expansion IRQ)</td>
</tr>
<tr>
<td>*CS2</td>
<td>16</td>
<td>RDY</td>
<td>0x0800.0000</td>
<td>0x0BFF.FFFF</td>
<td>Expansion Chip Select</td>
</tr>
<tr>
<td>*CS3</td>
<td>16</td>
<td>5</td>
<td>0x0C00.0000</td>
<td>0x0FFF.FFFF</td>
<td>LAN9211 Ethernet I/F</td>
</tr>
<tr>
<td>*CS4</td>
<td>32</td>
<td>RDY</td>
<td>0x1000.0000</td>
<td>0x13FF.FFFF</td>
<td>SM501</td>
</tr>
<tr>
<td>*CS5</td>
<td>8</td>
<td>10</td>
<td>0x1400.0000</td>
<td>0x17FF.FFFF</td>
<td>NAND Flash</td>
</tr>
<tr>
<td>*PCS0</td>
<td>N/A</td>
<td>N/A</td>
<td>0x2000.0000</td>
<td>0x2FFF.FFFF</td>
<td>Compact Flash Socket 0</td>
</tr>
<tr>
<td>*PCS1</td>
<td>N/A</td>
<td>N/A</td>
<td>0x3000.0000</td>
<td>0x3FFF.FFFF</td>
<td>Compact Flash Socket 1 (unused)</td>
</tr>
<tr>
<td>*SDCS0</td>
<td>32</td>
<td>N/A</td>
<td>0xA000.0000</td>
<td>0xA3FF.FFFF</td>
<td>128Mbyte SDRAM</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I2C</th>
<th>I2C Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C</td>
<td>N/A</td>
<td>0x58</td>
</tr>
</tbody>
</table>

Table 2 – CSB726 Address Map

4.1.1 ADDRESS MAP NOTES

1. Address ranges are based on the PXA270 maximum range for that chip select. The actual device or devices controlled by the chip select may not fill the range, but will repeat multiple times based on their actual size.

2. RDY in the “Wait States” column indicates the device uses the RDY input to the PXA270 to control the access. Wait States are based on the device access times assuming a 104Mhz bus clock.

3. *PCS0 and *PCS1 are not actual chip selects. They represent the space used by the PCMCIA/Compact Flash interface.

4. Software must program SDRAM Chip Select 0 (*SDCS0) for large
SDRAM operation in order to use the 128Mbyte SDRAM.

5. The DS1339 Address is the I2C address it responds to. Software must setup the PXA270 I2C Controller to access the DS1339.

### 4.2 64MBYTE SPANSION FLASH

The CSB726 uses a Spansion S29GL512N connected to *CS0 for boot memory. *CS0 is set to 16-bits width by hardware strapping and maximum wait states after reset. The access time of the Flash is 110ns. Initialization software should change the settings of *CS0 for optimal performance as soon as possible.

The Spansion S29GL512N also provides a unique 64-bit ID thus allowing for security and IP rights software to use this as a board identifier.

### 4.3 128MBYTE MOBILE SDRAM

The CSB726 uses two 32Mx16, PC133 Mobile SDRAM devices connected to *SDCS0 for system memory. The PXA270 memory controller should be programmed for 104Mhz, CAS Latency=2 and RAS to CAS=2 operation. Refer to the PXA270 User Manual for more information on programming the SDRAM Memory Controller, including the mobile and large SDRAM options.

### 4.4 512MBYTE 8-BIT NAND FLASH

The CSB726 has a single TSSOP, 8-Bit, 512Mbyte NAND Flash. This device is connected to PXA270 Chip Select 5.

The signals used to interface with the NAND Flash are shown in the following table.

<table>
<thead>
<tr>
<th>NAND Signal</th>
<th>PXA270 Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>*N_CE</td>
<td>*CS5</td>
<td>*N_CE is also driven low when PXA270 GPIO21 is low</td>
</tr>
<tr>
<td>*N_WE</td>
<td>*WE</td>
<td>Write Enable (Qualified with *CS5)</td>
</tr>
<tr>
<td>*N_RE</td>
<td>*OE</td>
<td>Read Enable (Qualified with *CS5)</td>
</tr>
<tr>
<td>N_ALE</td>
<td>A3</td>
<td>Addresses are latched on the rising edge of *N_WE when ALE = 1</td>
</tr>
<tr>
<td>N_CLE</td>
<td>A4</td>
<td>Commands are latched on the rising edge of *N_WE when CLE = 1</td>
</tr>
<tr>
<td>N_RDY</td>
<td>GPIO20</td>
<td>High indicates the NAND is ready for a new command</td>
</tr>
<tr>
<td>N_D0-7</td>
<td>D0-7</td>
<td>8-Bit Data bus, Addresses, Commands and Data are transferred via these signals</td>
</tr>
</tbody>
</table>
4.4.1 NAND FLASH NOTES

1. The NAND Flash is connected to *CS5 as an 8-bit wide device with 11 wait states minimum (105nsec at 104Mhz bus clock).

2. The NAND Flash used on the CSB726 might be a “CE Care” type. This means that prior to issuing certain commands, GPIO21 must be set low. This will insure that the *N_CE signal stays low until GPIO21 is set back high. This would be done, for example, on a page write or erase command. For “CE Don’t Care” devices this method will not cause any problem.

3. The PXA270 NAND Flash software should monitor GPIO20 to detect the completion of a NAND Flash operation (or alternately set GPIO20 as a high true interrupt input).

4. The Write Protect pin of the NAND Flash is tied high, so no Write Protect function is available.

5. Currently the CSB726 ships with a Samsung K9F4G08U0M (4Mbit, 512M x 8) device. Future products may ship with the same or larger capacity NAND device. Contact Cogent for updated information on the currently shipping NAND Flash.

4.5 SMSC LAN9211 ETHERNET CONTROLLER

The CSB726 uses the LAN9211 to provide a Low Power 10/100Mbit Ethernet Interface. This device is mapped to CPU Chip Select 3. In addition, the interrupt output of the LAN9211 is connected to CPU GPIO52.

The signals used to interface with the LAN9211 are shown in the following table.

<table>
<thead>
<tr>
<th>LAN9211 Signal</th>
<th>PXA270 Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>*RST</td>
<td>*RST_OUT</td>
<td>*N_CE is also driven low when PXA270 GPIO21 is low</td>
</tr>
<tr>
<td>*CS</td>
<td>*CS3</td>
<td>*N_CE is also driven low when PXA270 GPIO21 is low</td>
</tr>
<tr>
<td>*WE</td>
<td>*PWE</td>
<td>PCMCIA Write Enable (required for VLIO devices)</td>
</tr>
<tr>
<td>*RD</td>
<td>*OE</td>
<td>Output Enable</td>
</tr>
<tr>
<td>A1-A7</td>
<td>LA1-7</td>
<td>Register Addresses</td>
</tr>
<tr>
<td>FIFO_SEL</td>
<td>LA8</td>
<td>1 = TX/RX FIFO Select, 0 = I/O Registers Select</td>
</tr>
<tr>
<td>*IRQ</td>
<td>GPIO52</td>
<td>Set to Low True</td>
</tr>
</tbody>
</table>
4.5.1 LAN9211 INTERFACE NOTES

1. The LAN9211 is connected to *CS3 as a 16-bit wide device with 6 wait states minimum and VLIO enabled. Although the ready input to the PXA270 is not used, VLIO mode is required for proper read/write strobe timing.

2. The LAN9211 has restrictions in back to back accesses to certain registers. Refer to the LAN9211 documentation for more detail, but in general, there must be at least 135ns (15 clocks at 104Mhz) from one read to the next read or write.

3. GPIO52 is connected to the LAN9211 Interrupt (*IRQ). The LAN9211 Interrupt is a low true, level output.

4. The twisted pair signals from the LAN9211 are routed to SODIMM signals E_TDX, E_TXD+, E_RXD+ and E_RXD-. They are designed to connect to a 10/100 compatible transformer with the transformer center tap connected to VCC3 and bypassed to ground with a .1uf capacitor. These signals should be routed differentially (100 ohm impedance) and separated from other signals by at least 25mils. The total length should be kept to 2” or less.

5. LAN9211 LED outputs *LED_SPD and *LED_LNK are routed to the SODIMM signals *E_SPD and *E_LNK respectively. They should be programmed by software to be low true. Also, the *LED_LNK signal should be programmed to blink off during transmit or receive activity.

4.6 SM501 2D GRAPHICS COPROCESSOR

The SM501 (or the SM502, a drop-in replacement) provides the CSB726 with a high performance, low power LCD controller as well as several peripheral functions. These are described in the following subsections.

4.6.1 SM501 INTERFACE NOTES

1. The SM501 Chip Select is connected to *CS4. Software must initialize this chip select for 32-Bit, VLIO operation with external ready.

2. The SM501 interrupt is connected to PXA270 GPIO53. It is a low true, level interrupt.

3. The SM501 has 8Mbyte of Internal Frame Buffer starting at address 0x1000 0000. This places the internal SM501 registers at address 0x13E0 0000.
4. The SM501 on the CSB726 uses a 24Mhz crystal. Refer to the SM501 Users Manual for information regarding clocking and power control when using a 24Mhz crystal.

4.6.2 SM501 2D GRAPHICS CONTROLLER
The SM501 contains a 2D Graphics accelerator supporting various functions such as: Line Draw; Polygon draw and fill; Block Move; and Line Clipping. This controller operates on the internal 8Mbyte frame buffer memory and has no associated external signals.

4.6.3 SM501 LCD PANEL INTERFACE
The primary function of the SM501 is to provide output to an external LCD panel. The SM501 supports 1, 2, 4, 8, 16 and 24 Bits per pixel (BPP). 18-Bits are routed to the SODIMM connector. The CSB726 can support up to 1024 x 768 resolution.

The signals used to interface the SM501 LCD Output to the SODIMM LCD Port are shown in the following table.

<table>
<thead>
<tr>
<th>SM501 Signal</th>
<th>SODIMM Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>FP_D18</td>
<td>LCD_R0</td>
<td>Red Bit 0 (LSB)</td>
</tr>
<tr>
<td>FP_D19</td>
<td>LCD_R1</td>
<td>Red Bit 1</td>
</tr>
<tr>
<td>FP_D20</td>
<td>LCD_R2</td>
<td>Red Bit 2</td>
</tr>
<tr>
<td>FP_D21</td>
<td>LCD_R3</td>
<td>Red Bit 3</td>
</tr>
<tr>
<td>FP_D22</td>
<td>LCD_R4</td>
<td>Red Bit 4</td>
</tr>
<tr>
<td>FP_D23</td>
<td>LCD_R5</td>
<td>Red Bit 5</td>
</tr>
<tr>
<td>FP_D10</td>
<td>LCD_G0</td>
<td>Green Bit 0</td>
</tr>
<tr>
<td>FP_D11</td>
<td>LCD_G1</td>
<td>Green Bit 1</td>
</tr>
<tr>
<td>FP_D12</td>
<td>LCD_G2</td>
<td>Green Bit 2</td>
</tr>
<tr>
<td>FP_D13</td>
<td>LCD_G3</td>
<td>Green Bit 3</td>
</tr>
<tr>
<td>FP_D14</td>
<td>LCD_G4</td>
<td>Green Bit 4</td>
</tr>
<tr>
<td>FP_D15</td>
<td>LCD_G5</td>
<td>Green Bit 5</td>
</tr>
<tr>
<td>FP_D2</td>
<td>LCD_B0</td>
<td>Blue Bit 0</td>
</tr>
<tr>
<td>FP_D3</td>
<td>LCD_B1</td>
<td>Blue Bit 1</td>
</tr>
<tr>
<td>FP_D4</td>
<td>LCD_B2</td>
<td>Blue Bit 1</td>
</tr>
</tbody>
</table>
The SM501 Primary Signal | SM501 Secondary Signal | SODIMM Signal
---|---|---
VIP_D0 | ZV0/GPIO16 | U0_TXD/GPIO37
VIP_D1 | ZV0/GPIO17 | U0_RXD/GPIO38
VIP_D2 | ZV0/GPIO18 | U0_RTS/GPIO40
VIP_D3 | ZV0/GPIO19 | U0_CTS/GPIO39
VIP_D4 | ZV0/GPIO20 | U0_TXD/SSP1_TXD/GPIO41

Table 5 – SM501 to LCD Connections

4.6.4 SM501 LCD NOTES

5. LCD_BKL is connected to SM501 GPIO30/PWM1. This allows the LCD backlight to be controlled in PWM mode if desired. Refer to the appropriate documentation to see if PWM mode is supported by the attached LCD backlight power supply (on the CSB702 it is).

4.6.5 ZV VIDEO INPUT PORT

The SM501 has an 8 or 16-Bit video input port. The CSB726 supports 8-bit mode. Video input can be in YUV4:2:2 or CCIR656 format. Note that these signals are connected on the CSB726 to other SM501 peripherals. It is the responsibility of software to initialize the SM501 peripherals for the desired mode of operation. For example, if ZV input is not used then those signals should be initialized as GPIO inputs to prevent conflict with the other peripherals.

The following table describes the peripheral multiplexing for the SM501 ZV port.

VIP_D0 | ZV0/GPIO16 | U0_TXD/GPIO37
VIP_D1 | ZV0/GPIO17 | U0_RXD/GPIO38
VIP_D2 | ZV0/GPIO18 | U0_RTS/GPIO40
VIP_D3 | ZV0/GPIO19 | U0_CTS/GPIO39
VIP_D4 | ZV0/GPIO20 | U0_TXD/SSP1_TXD/GPIO41
VIP_D5   ZV0/GPIO21   U0_RXD/ SSP1_RXD/GPIO42
VIP_D6   ZV0/GPIO22   U0_RTS/ SSP1_FRMOUT/GPIO44
VIP_D7   ZV0/GPIO23   U0_CTS/ SSP1_FRMIN/GPIO43
VIP_D8   N/A   PWM0/GPIO29
VIP_D9   N/A   PWM2/GPIO31
VIP_HSYNC   VP_HREF   I2C_SDA
VIP_VSYNC   VP_VSYNC   I2C_SCL
VIP_PCLK   VP_CLK   SSP1_CLK/GPIO45

Table 6 – SM501 Peripheral Multiplexing

4.6.6 SM501 UARTS, SSP AND I2C
The SM501 has two 4-wire UARTS, two SSP ports and one I2C port. Both UARTS, one of the SSP ports (SSP1 which is shared with UART1) and the I2C port are made available on the SODIMM VIP pins as shown in Table 6. To use the alternate signals, the ZV video port should be disabled to prevent false interrupts. Also, UART1 and SSP1 share the same SM501 pins and software must select the desired mode of operation.

4.7 SM501 UNAVAILABLE PORTS
The following SM501 ports are not available on the CSB726: CRT; Upper ZV input bits 8-15; SSP0; AC97/I2S Audio; USB 1.1; and any GPIO not defined.

4.8 DS1339 RTC
A Maxim DS1339 provides a battery backed Real Time Clock function. It is on the PXA270 I2C Bus at I2C address 0x58. It is expected that software will transfer the current time value from the DS1339 to the PXA270 internal RTC function at power up and update the DS1339 when the PXA270 RTC is changed. The DS1339 offer superior current consumption (<1 microamp) compared to the PXA270 RTC internal function (~40 microamps). A standard 48ma/hr coin cell (CR2032) will power the DS1339 for ~3 years across the full temperature range versus ~20 days for the PXA270 internal RTC.

The signals used to interface with the DS1339 are shown in the following table.

<table>
<thead>
<tr>
<th>DS1339 Signal</th>
<th>PXA270 Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCL</td>
<td>GPIO117/SCL</td>
<td>I2C Bus Clock</td>
</tr>
</tbody>
</table>
4.8.1 DS1339 RTC INTERFACE NOTES

1. The DS1339 SQW output is used to provide the PXA270 32.768Khz clock. By default this signal is enabled. Software must not change the settings for this output even if the PXA270 internal RTC is not used. This is because the 32.768Khz input is used by the PXA270 power management functions as well as by the RTC function.

2. The DS1339 is powered from the main 3.3V rail when present. This will reduce the current draw on the battery to less than 0.1 microamps.

3. The DS1339 has a provision for a rechargeable coin cell. This is not supported on the CSB726 and must not be enabled.

4.9 LM3489 3.3V REGULATOR

A National Semiconductor LM3489 wide input switching regulator provides the CSB726, and optionally the rest of the system, with the main 3.3V rail. The input voltage can be from 6V to a maximum of 35V, though it is optimized for 9V to 15V operation for peak efficiency and maximum current output. However, across the entire input voltage range, the current output of this regulator is 4 Amps minimum. The CSB726 requires up to 2 Amps peak, leaving 2 Amps minimum for the rest of the system.

4.9.1 LM3489 3.2V REGULATOR NOTES

4. The LM3489 is disabled when the SODIMM signal *PWR_DIS is low. *PWR_DIS must be floated to enable the LM3489 (not driven high).

5. The SODIMM VIN Mounting Hole supplies the input to the LM3489 while the SODIMM VCC3 Mounting Hole provides the 3.3V to the system.

4.10 ISL6271 CORE VOLTAGE REGULATOR

An Intersil ISL6271 multi-output regulator is used to provide the core and other voltages to the PXA270. The ISL6271 is powered from the main 3.3V rail. The ISL6271 may be controlled via the PXA270 SMBUS using PWR_SCL and PWR_SDA. The SMBUS can be used to set the ISL6271 output voltage during PXA270 operation, thus allowing software to implement DVFS (Dynamic Voltage and Frequency Scaling). Refer to the PXA270 Users Manual and the ISL6271 Data Sheet for detailed programming information.
4.10.1 ISL6271 CORE REGULATOR NOTES

6. The ISL6271 is configured via hardware strapping for SMBUS mode to allow DVFS operation. The ISL6271 core voltage output defaults to 1.5V. If DVFS is not desired, then the SMBUS interface is not used.

7. The SMBUS signals are PXA270 PWR_SCL and PWR_SDA.

8. The PXA270 signal PWREN, also routed to the SODIMM as the signal *LOW_PWR, is used to enable/disable the ISL6271.
5 PXA270 ON-CHIP PERIPHERALS

5.1 OVERVIEW
The PXA270 has a number of on-chip peripheral devices as well as a large number of user defined GPIOs. While it is beyond the scope of this document to provide detailed programming and interfacing information for the PXA270 on-chip peripherals, the following section describes the assignments for these devices and GPIOs as they are implemented on the CSB726.

5.2 PXA270 TO SODIMM PERIPHERAL MAPPING
The following table provides a high level view of the mapping from the various PXA270 peripherals to the SODIMM ports.

<table>
<thead>
<tr>
<th>PXA270 Peripheral</th>
<th>SODIMM Port</th>
<th>Description and Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSP1</td>
<td>SSI</td>
<td>SSP1 may be used in SPI or I2S mode</td>
</tr>
<tr>
<td>SSP2</td>
<td>SPI0</td>
<td>SSP2 must be programmed to SPI mode</td>
</tr>
<tr>
<td>SSP3</td>
<td>SPI1</td>
<td>SSP3 must be programmed to SPI mode</td>
</tr>
<tr>
<td>AC97</td>
<td>AC97/I2S</td>
<td>AC97 Codec Interface</td>
</tr>
<tr>
<td>FF UART</td>
<td>UART0</td>
<td>DCD, DTR, DSR and RI are routed to UART2</td>
</tr>
<tr>
<td>BT UART</td>
<td>UART1</td>
<td>Provides RTS and CTS handshaking</td>
</tr>
<tr>
<td>STD UART</td>
<td>DBG</td>
<td>TXD/RXD via on-board RS232 buffer</td>
</tr>
<tr>
<td>LCD</td>
<td>-</td>
<td>The PXA270 LCD I/F is not available</td>
</tr>
<tr>
<td>CIF</td>
<td>-</td>
<td>The PXA270 Camera I/F is not available</td>
</tr>
<tr>
<td>KEYPAD</td>
<td>GPIO6-9</td>
<td>Only KP_DKIN1-4 are available</td>
</tr>
<tr>
<td>SD/MMC</td>
<td>SD/MMC 0</td>
<td>4-Bit SDIO compatible</td>
</tr>
<tr>
<td>PCMCIA</td>
<td>CF</td>
<td>Compact Flash Interface</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C</td>
<td>I2C Bus</td>
</tr>
<tr>
<td>PWR_I2C</td>
<td>-</td>
<td>Used to connect to Core Switching Regulator</td>
</tr>
<tr>
<td>USB HOST 0</td>
<td>USB HOST 0</td>
<td>USB 1.1 Host Port 0</td>
</tr>
<tr>
<td>USB DEVICE</td>
<td>USB DEVICE</td>
<td>May be used as USB 1.1 Host 1</td>
</tr>
<tr>
<td>SIM</td>
<td>-</td>
<td>PXA270 SIM I/F is not available</td>
</tr>
</tbody>
</table>
### 5.3 PXA270 CHIP SELECTS

As described in Section 4.1, the PXA270 Chip Selects are used to enable the various peripheral devices on the CSB726 as well as expansion devices via the SODIMM connector. As a cross-reference they are described again in the following table.

<table>
<thead>
<tr>
<th>Chip Select</th>
<th>Attached Device(s)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>*CS0</td>
<td>S29GL512N Spansion Flash</td>
<td>16-Bit non-VLIO, Boot Device</td>
</tr>
<tr>
<td>*CS1</td>
<td>Used as GPIO15 (Expansion IRQ)</td>
<td>SODIMM *EXP_IRQ</td>
</tr>
<tr>
<td>*CS2</td>
<td>Expansion Chip Select</td>
<td>16-Bit VLIO with RDY</td>
</tr>
<tr>
<td>*CS3</td>
<td>LAN9211</td>
<td>16-Bit VLIO no RDY</td>
</tr>
<tr>
<td>*CS4</td>
<td>SM501</td>
<td>32-Bit VLIO with RDY</td>
</tr>
<tr>
<td>*CS5</td>
<td>NAND Flash</td>
<td>8-Bit non-VLIO</td>
</tr>
<tr>
<td>*PCS0</td>
<td>Compact Flash Socket 0</td>
<td>PCMCIA/CF Socket 0</td>
</tr>
<tr>
<td>*PCS1</td>
<td>Compact Flash Socket 1 (unused)</td>
<td>PCMCIA/CF Socket 1</td>
</tr>
</tbody>
</table>

Table 9 – PXA270 Chip Select Assignments

### 5.4 PXA270 GENERAL PURPOSE I/O ASSIGNMENTS

The PXA270 has 119 General Purpose I/O bits (0 to 118). The GPIO usage on the CSB726 is described in the following table. It is the responsibility of software to setup these bits for the correct direction and default state as well as the assignment of alternate functions.

<table>
<thead>
<tr>
<th>PXA270 GPIO</th>
<th>DIR</th>
<th>CSB726 Usage</th>
<th>ALT FUNC</th>
<th>Description and Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>N/A</td>
<td>N/A</td>
<td>0</td>
<td>GPIO0 is not available on the CSB726</td>
</tr>
<tr>
<td>1</td>
<td>I/O</td>
<td>GPIO0</td>
<td>0</td>
<td>SODIMM GPIO0/IRQ</td>
</tr>
<tr>
<td>2</td>
<td>N/A</td>
<td>N/A</td>
<td>0</td>
<td>Not Available on PXA270</td>
</tr>
<tr>
<td>PXA270 GPIO</td>
<td>DIR</td>
<td>CSB726 GPIO Usage</td>
<td>ALT FUNC</td>
<td>Description and Notes</td>
</tr>
<tr>
<td>------------</td>
<td>-----</td>
<td>-------------------</td>
<td>---------</td>
<td>------------------------------------------</td>
</tr>
<tr>
<td>3</td>
<td>I/O</td>
<td>PWR_SCL</td>
<td>0</td>
<td>ISL6271 SMBUS Clock</td>
</tr>
<tr>
<td>4</td>
<td>I/O</td>
<td>PWR_SDA</td>
<td>0</td>
<td>ISL6271 SMBUS Data</td>
</tr>
<tr>
<td>5-8</td>
<td>N/A</td>
<td>N/A</td>
<td>0</td>
<td>Not Available on PXA270</td>
</tr>
<tr>
<td>9</td>
<td>I/O</td>
<td>GPIO2</td>
<td>0</td>
<td>SODIMM GPIO2/TMR</td>
</tr>
<tr>
<td>10</td>
<td>I/O</td>
<td>GPIO3</td>
<td>0</td>
<td>SODIMM GPIO3/TMR</td>
</tr>
<tr>
<td>11</td>
<td>I/O</td>
<td>GPIO1</td>
<td>0</td>
<td>SODIMM GPIO1/IRQ</td>
</tr>
<tr>
<td>12</td>
<td>IN</td>
<td>*PIIRQ</td>
<td>0</td>
<td>Touch Controller Interrupt</td>
</tr>
<tr>
<td>13</td>
<td>OUT</td>
<td>SPI0_MOSI</td>
<td>1</td>
<td>PXA270 SSP2 Transmit</td>
</tr>
<tr>
<td>14</td>
<td>OUT</td>
<td>*SPI0_CS0</td>
<td>2</td>
<td>PXA270 SSP2 Frame</td>
</tr>
<tr>
<td>15</td>
<td>IN</td>
<td>*EXP_IRQ</td>
<td>0</td>
<td>Expansion Interrupt</td>
</tr>
<tr>
<td>16</td>
<td>I/O</td>
<td>GPIO4</td>
<td>0</td>
<td>SODIMM GPIO4/PWM</td>
</tr>
<tr>
<td>17</td>
<td>I/O</td>
<td>GPIO5</td>
<td>0</td>
<td>SODIMM GPIO5/PWM</td>
</tr>
<tr>
<td>18</td>
<td>IN</td>
<td>*EXP_WAIT</td>
<td>0</td>
<td>*EXP_WAIT (PXA270 RDY)</td>
</tr>
<tr>
<td>19</td>
<td>OUT</td>
<td>SPI0_CLK</td>
<td>1</td>
<td>PXA270 SSP2 Clock</td>
</tr>
<tr>
<td>20</td>
<td>IN</td>
<td>N_RDY</td>
<td>0</td>
<td>NAND Flash RDY/*BSY signal</td>
</tr>
<tr>
<td>21</td>
<td>OUT</td>
<td>NGPIO</td>
<td>0</td>
<td>Drives NAND Flash *N_CE low when 0</td>
</tr>
<tr>
<td>22</td>
<td>IN</td>
<td>SPI0_RDY</td>
<td>1</td>
<td>SPI0 ready (or external clock for SPI0)</td>
</tr>
<tr>
<td>23</td>
<td>I/O</td>
<td>SSI_CLK</td>
<td>2</td>
<td>PXA270 SSP1 Clock</td>
</tr>
<tr>
<td>24</td>
<td>I/O</td>
<td>SSI_FRM</td>
<td>2</td>
<td>PXA270 SSP1 Frame</td>
</tr>
<tr>
<td>25</td>
<td>OUT</td>
<td>SSI_TXD</td>
<td>2</td>
<td>PXA270 SSP1 Transmit</td>
</tr>
<tr>
<td>26</td>
<td>IN</td>
<td>SSI_RXD</td>
<td>1</td>
<td>PXA270 SSP1 Receive</td>
</tr>
<tr>
<td>27</td>
<td>I/O</td>
<td>SSI_EXTCLK</td>
<td>1</td>
<td>PXA270 SSP1 External Clock</td>
</tr>
<tr>
<td>28</td>
<td>IN</td>
<td>AC_BCLK</td>
<td>1</td>
<td>AC97 Bit Clock from Codec</td>
</tr>
<tr>
<td>29</td>
<td>IN</td>
<td>AC_SDIN</td>
<td>1</td>
<td>AC97 Serial Data from Codec</td>
</tr>
<tr>
<td>30</td>
<td>OUT</td>
<td>AC_SDOUT</td>
<td>2</td>
<td>AC97 Serial Data to Codec</td>
</tr>
<tr>
<td>31</td>
<td>OUT</td>
<td>AC_SYNC</td>
<td>2</td>
<td>AC97 Frame Sync to Codec</td>
</tr>
<tr>
<td>32</td>
<td>OUT</td>
<td>SD_CLK</td>
<td>2</td>
<td>SD/MMC Clock</td>
</tr>
<tr>
<td>33</td>
<td>OUT</td>
<td>*CS5</td>
<td>2</td>
<td>NAND Flash</td>
</tr>
<tr>
<td>PXA270 GPIO</td>
<td>DIR</td>
<td>CSB726 Usage</td>
<td>ALT FUNC</td>
<td>Description and Notes</td>
</tr>
<tr>
<td>------------</td>
<td>-----</td>
<td>--------------</td>
<td>----------</td>
<td>-----------------------</td>
</tr>
<tr>
<td>34</td>
<td>IN</td>
<td>U0_RXD</td>
<td>1</td>
<td>PXA270 FFUART Receive Data</td>
</tr>
<tr>
<td>35</td>
<td>IN</td>
<td>U0_CTS</td>
<td>1</td>
<td>PXA270 FFUART Clear To Send</td>
</tr>
<tr>
<td>36</td>
<td>IN</td>
<td>U0_DCD</td>
<td>1</td>
<td>PXA270 FFUART Data Carrier Detect</td>
</tr>
<tr>
<td>37</td>
<td>IN</td>
<td>U0_DSR</td>
<td>1</td>
<td>PXA270 FFUART Data Set Ready</td>
</tr>
<tr>
<td>38</td>
<td>IN</td>
<td>U0_RI</td>
<td>1</td>
<td>PXA270 FFUART Ring</td>
</tr>
<tr>
<td>39</td>
<td>OUT</td>
<td>U0_TXD</td>
<td>2</td>
<td>PXA270 FFUART Transmit Data</td>
</tr>
<tr>
<td>40</td>
<td>OUT</td>
<td>U0_DTR</td>
<td>2</td>
<td>PXA270 FFUART Data Terminal Ready</td>
</tr>
<tr>
<td>41</td>
<td>OUT</td>
<td>U0_RTS</td>
<td>2</td>
<td>PXA270 FFUART Request To Send</td>
</tr>
<tr>
<td>42</td>
<td>IN</td>
<td>U1_RXD</td>
<td>1</td>
<td>PXA270 BTUART Receive Data</td>
</tr>
<tr>
<td>43</td>
<td>OUT</td>
<td>U1_TXD</td>
<td>2</td>
<td>PXA270 BTUART Transmit Data</td>
</tr>
<tr>
<td>44</td>
<td>IN</td>
<td>U1_CTS</td>
<td>1</td>
<td>PXA270 BTUART Clear To Send</td>
</tr>
<tr>
<td>45</td>
<td>OUT</td>
<td>U1_RTS</td>
<td>2</td>
<td>PXA270 BTUART Request To Send</td>
</tr>
<tr>
<td>46</td>
<td>IN</td>
<td>DBG_RXD</td>
<td>2</td>
<td>RS232 Debug Receive Data (PXA270 STDUART)</td>
</tr>
<tr>
<td>47</td>
<td>OUT</td>
<td>DBG_TXD</td>
<td>1</td>
<td>RS232 Debug Transmit Data (PXA270 STDUART)</td>
</tr>
<tr>
<td>48</td>
<td>OUT</td>
<td>*CF_OE</td>
<td>2</td>
<td>Compact Flash Memory Output Enable</td>
</tr>
<tr>
<td>49</td>
<td>OUT</td>
<td>*CF_WE</td>
<td>2</td>
<td>Compact Flash Memory Write Enable</td>
</tr>
<tr>
<td>50</td>
<td>OUT</td>
<td>*CF_IOR</td>
<td>2</td>
<td>Compact Flash I/O Read Enable</td>
</tr>
<tr>
<td>51</td>
<td>OUT</td>
<td>*CF_IOW</td>
<td>2</td>
<td>Compact Flash I/O Write Enable</td>
</tr>
<tr>
<td>52</td>
<td>IN</td>
<td>*E_INT</td>
<td>0</td>
<td>LAN9211 Interrupt, Low True</td>
</tr>
<tr>
<td>53</td>
<td>IN</td>
<td>*SM_INT</td>
<td>0</td>
<td>SM501 Interrupt, Low True</td>
</tr>
<tr>
<td>54</td>
<td>OUT</td>
<td>*CF_CE2</td>
<td>2</td>
<td>Compact Flash Chip Enable 2</td>
</tr>
<tr>
<td>55</td>
<td>OUT</td>
<td>*CF_REG</td>
<td>2</td>
<td>Compact Flash Register Select</td>
</tr>
<tr>
<td>56</td>
<td>IN</td>
<td>*CF_WAIT</td>
<td>1</td>
<td>Compact Flash Wait Request</td>
</tr>
<tr>
<td>57</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>PCMCIA *IOIS16 - Not Used</td>
</tr>
<tr>
<td>58-77</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>PXA270 LCD Controller signals – Not Used</td>
</tr>
<tr>
<td>78</td>
<td>OUT</td>
<td>*EXP_CS</td>
<td>2</td>
<td>SODIMM Expansion Chip Select (*CS2)</td>
</tr>
<tr>
<td>79</td>
<td>OUT</td>
<td>*E_CS</td>
<td>2</td>
<td>LAN9211 Chip Select (*CS3)</td>
</tr>
<tr>
<td>PXA270 GPIO</td>
<td>DIR</td>
<td>CSB726 Usage</td>
<td>ALT FUNC</td>
<td>Description and Notes</td>
</tr>
<tr>
<td>------------</td>
<td>-----</td>
<td>-------------</td>
<td>---------</td>
<td>-----------------------</td>
</tr>
<tr>
<td>80</td>
<td>OUT</td>
<td>*SM_CS</td>
<td>2</td>
<td>SM501 Chip Select (*CS4)</td>
</tr>
<tr>
<td>81</td>
<td>OUT</td>
<td>*SPI1_MOSI</td>
<td>1</td>
<td>PXA270 SSP3 Transmit</td>
</tr>
<tr>
<td>82</td>
<td>IN</td>
<td>*SPI1_MISO</td>
<td>1</td>
<td>PXA270 SSP3 Receive</td>
</tr>
<tr>
<td>83</td>
<td>OUT</td>
<td>*SPI1_CS0</td>
<td>1</td>
<td>PXA270 SSP3 Frame</td>
</tr>
<tr>
<td>84</td>
<td>OUT</td>
<td>SPI1_CLK</td>
<td>1</td>
<td>SPI1 Clock</td>
</tr>
<tr>
<td>85</td>
<td>OUT</td>
<td>*CF_CE1</td>
<td>1</td>
<td>Compact Flash Chip Enable 1</td>
</tr>
<tr>
<td>86</td>
<td>IN</td>
<td>SPI0_MISO</td>
<td>1</td>
<td>PXA270 SSP2 Receive</td>
</tr>
<tr>
<td>87</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>88</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>89</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>90</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>91</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>92</td>
<td>I/O</td>
<td>SD0_D0</td>
<td>1</td>
<td>SD/MMC Data Bit 0</td>
</tr>
<tr>
<td>93</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>94</td>
<td>I/O</td>
<td>GPIO6</td>
<td>0</td>
<td>SODIMM GPIO6</td>
</tr>
<tr>
<td>95</td>
<td>I/O</td>
<td>GPIO7</td>
<td>0</td>
<td>SODIMM GPIO7</td>
</tr>
<tr>
<td>96</td>
<td>I/O</td>
<td>GPIO8</td>
<td>0</td>
<td>SODIMM GPIO8</td>
</tr>
<tr>
<td>97</td>
<td>I/O</td>
<td>GPIO9</td>
<td>0</td>
<td>SODIMM GPIO9</td>
</tr>
<tr>
<td>98</td>
<td>IN</td>
<td>CF_RDY</td>
<td>0</td>
<td>Compact Flash Card Ready/Busy and IRQ</td>
</tr>
<tr>
<td>99</td>
<td>IN</td>
<td>*CF_CD</td>
<td>0</td>
<td>Compact Flash Card Detect (0 = card in)</td>
</tr>
<tr>
<td>100</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>101</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>102</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>103</td>
<td>OUT</td>
<td>CF_RST</td>
<td>0</td>
<td>Compact Flash Reset, Active High</td>
</tr>
<tr>
<td>104</td>
<td>IN</td>
<td>*I2C_INT</td>
<td>0</td>
<td>Shared Interrupt from I2C devices</td>
</tr>
<tr>
<td>105</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>106</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>107</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
</tbody>
</table>
### Table 10 – PXA270 GPIO Pin Assignments

<table>
<thead>
<tr>
<th>PXA270 GPIO</th>
<th>DIR</th>
<th>CSB726 Usage</th>
<th>ALT FUNC</th>
<th>Description and Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>108</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>109</td>
<td>I/O</td>
<td>SD0_D1</td>
<td>1</td>
<td>SD/MMC Data Bit 1</td>
</tr>
<tr>
<td>110</td>
<td>I/O</td>
<td>SD0_D2</td>
<td>1</td>
<td>SD/MMC Data Bit 2</td>
</tr>
<tr>
<td>111</td>
<td>I/O</td>
<td>SD0_D3</td>
<td>1</td>
<td>SD/MMC Data Bit 3</td>
</tr>
<tr>
<td>112</td>
<td>OUT</td>
<td>SD0_CMD</td>
<td>1</td>
<td>SD/MMC Command</td>
</tr>
<tr>
<td>113</td>
<td>OUT</td>
<td>*AC_RST</td>
<td>2</td>
<td>AC97 Reset to Codec</td>
</tr>
<tr>
<td>114</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>115</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>116</td>
<td>OUT</td>
<td>0</td>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td>117</td>
<td>I/O</td>
<td>I2C_SCL</td>
<td></td>
<td>I2C Clock</td>
</tr>
<tr>
<td>118</td>
<td>I/O</td>
<td>I2C_SDA</td>
<td></td>
<td>I2C Data</td>
</tr>
</tbody>
</table>

### 5.4.1 PXA270 GPIO NOTES

9. An asterisk (ie *PIRQ) before a signal indicates that it is a low true signal.

10. The SODIMM interface defines 10 GPIO’s, numbered GPIO0 to GPIO9. Some of these have a preferred usage such as GPIO1/IRQ, which is used as an interrupt. This preference is not required and must be programmed by software to be used.

11. Signals indicated by N/A are not available.

12. Unused PXA270 GPIO must be programmed as outputs and set to 0 to insure the lowest noise and power consumption. These are indicated with an OUT in the direction column and a 0 in the usage column.

13. All SODIMM inputs should be tied to VCC3 or GND with a 10K ohm resistor on the target board. Do not leave unconnected.

14. The “ALT FUNC” column defines what Alternate Function should be programmed in order to get the stated functionality. 0 indicates an assignment to GPIO.

15. The PXA270 Users Manual shows GPIO’s 119 and 120. These are not available with the package used on the CSB726.
### 5.5 PXA270 INTERRUPT PIN ASSIGNMENTS

The PXA270 has a number of GPIO’s that are used as interrupt inputs to the Advanced Interrupt Controller. The following table describes the GPIO that are, or can be, used as interrupts on the CSB726. The SODIMM GPIO0 and GPIO1 are shown with the preferred use, but user software is required to enable the interrupt function for any signal.

<table>
<thead>
<tr>
<th>PXA270 GPIO</th>
<th>CSB726 Usage</th>
<th>Description and Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GPIO0</td>
<td>General Purpose I/O or Interrupt from Target Board</td>
</tr>
<tr>
<td>11</td>
<td>GPIO1</td>
<td>General Purpose I/O or Interrupt from Target Board</td>
</tr>
<tr>
<td>12</td>
<td>*PIRQ</td>
<td>Touch Controller Interrupt, Low True</td>
</tr>
<tr>
<td>15</td>
<td>*EXP_IRQ</td>
<td>Expansion Interrupt</td>
</tr>
<tr>
<td>20</td>
<td>N_RDY</td>
<td>NAND Flash Ready, High True</td>
</tr>
<tr>
<td>52</td>
<td>*E_INT</td>
<td>LAN9211 Interrupt, Low True</td>
</tr>
<tr>
<td>53</td>
<td>*SM_INT</td>
<td>SM501 Interrupt, Low True</td>
</tr>
<tr>
<td>98</td>
<td>CF_RDY</td>
<td>Compact Flash Card Ready (Memory Mode), High True or Compact Flash Card Interrupt (I/O Mode), High True</td>
</tr>
<tr>
<td>99</td>
<td>*CF_CD</td>
<td>Compact Flash Card Detect (0 = card inserted)</td>
</tr>
<tr>
<td>104</td>
<td>*I2C_INT</td>
<td>Shared I2C Interrupt, Low True</td>
</tr>
</tbody>
</table>

Table 11 – PXA270 Interrupt Pin Assignments

### 5.6 PXA270 UARTS

The PXA270 has 3 available UARTS. They are the Full Function (FF), Standard (STD) and Bluetooth (BT). The FF and STD UARTS support up to 230KBbps asynchronous serial communications, while the BT UART supports up to 921KBps. The STD UART is buffered with an RS-232 transceiver on the CSB726 and brought to the SODIMM as DBG_TXD and DBG_RXD. Refer to the PXA270 Users Manual for more information about the various PXA270 UARTS.

The signals used to interface the PXA270 UARTS to the SODIMM are shown in the following table.

<table>
<thead>
<tr>
<th>PXA270 Signal</th>
<th>SODIMM Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO39/FF_TXD</td>
<td>U0_TXD</td>
<td>UART0 Transmit Data</td>
</tr>
<tr>
<td>PXA270 Signal</td>
<td>SODIMM Signal</td>
<td>Notes</td>
</tr>
<tr>
<td>--------------</td>
<td>--------------</td>
<td>-------</td>
</tr>
<tr>
<td>GPIO34/FF_RXD</td>
<td>U0_RXD</td>
<td>UART0 Receive Data</td>
</tr>
<tr>
<td>GPIO41/FF_RTS</td>
<td>U0_RTS</td>
<td>UART0 Request To Send</td>
</tr>
<tr>
<td>GPIO35/FF_CTS</td>
<td>U0_CTS</td>
<td>UART0 Clear To Send</td>
</tr>
<tr>
<td>GPIO42/BT_TXD</td>
<td>U1_TXD</td>
<td>UART1 Transmit Data</td>
</tr>
<tr>
<td>GPIO43/BT_RXD</td>
<td>U1_RXD</td>
<td>UART1 Receive Data</td>
</tr>
<tr>
<td>GPIO45/BT_RTS</td>
<td>U1_RTS</td>
<td>UART1 Request To Send</td>
</tr>
<tr>
<td>GPIO44/BT_CTS</td>
<td>U1_CTS</td>
<td>UART1 Clear To Send</td>
</tr>
<tr>
<td>GPIO40/FF_DTR</td>
<td>U2_TXD/U0_DTR</td>
<td>UART2 Transmit Data or UART0 Data Transfer Request</td>
</tr>
<tr>
<td>GPIO37/FF_DSR</td>
<td>U2_RXD/U0_DSR</td>
<td>UART2 Receive Data or Data Set Ready</td>
</tr>
<tr>
<td>GPIO36/FF_DCD</td>
<td>U2_RTS/U0_DCD</td>
<td>UART2 Request To Send or UART0 Data Carrier Detect</td>
</tr>
<tr>
<td>GPIO38/FF_RI</td>
<td>U2_CTS/U0_RI</td>
<td>UART2 Clear To Send or UART0 Ring Indicator</td>
</tr>
<tr>
<td>GPIO/STD_TXD</td>
<td>DBG_TXD</td>
<td>Debug Transmit Data (RS232)</td>
</tr>
<tr>
<td>GPIO/STD_RXD</td>
<td>DBG_RXD</td>
<td>Debug Receive Data (RS232)</td>
</tr>
</tbody>
</table>

Table 12 – PXA270 UARTS to SODIMM Connections

5.6.1 PXA270 UART NOTES

1. All PXA270 UARTS support Standard Infrared (SIR) up to 115Kbits/s.

2. The PXA270 Fast IrDA UART shares it’s pins with the STD UART and thus is not available on the CSB726 (the RS232 transceiver is limited to 115Kbits/s).

5.7 PXA270 SSP/SPI CONTROLLERS
The PXA270 provides three high-speed Synchronous Serial Ports (SSP) controllers. SSP1, SSP2 and SSP3 are available on the SODIMM as SSP, SPI0 and SPI1 respectively. They are identical with the exception of no external clock option on SSP3 (SODIMM SPI1). Each controller can interface with SPI and Micro-wire slaves with minimal host intervention. The internal PXA270 DMA controller can be used to transfer data between the SSP controllers and system memory for high data rates (up to 13Mbits/sec. Refer to the PXA270 Users Manual for detailed programming information.
The signals used to interface the PXA270 SSP controllers to the SODIMM are shown in the following table.

<table>
<thead>
<tr>
<th>PXA270 Signal</th>
<th>SODIMM Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO23/SSP1_CLK</td>
<td>SSI_CLK</td>
<td>SSP Clock</td>
</tr>
<tr>
<td>GPIO24/SSP1_FRM</td>
<td>SSI_FRM</td>
<td>SSP Frame Sync</td>
</tr>
<tr>
<td>GPIO25/SSP1_TXD</td>
<td>SSI_TXD</td>
<td>SSP Transmit Data</td>
</tr>
<tr>
<td>GPIO26/SSP1_RXD</td>
<td>SSI_RXD</td>
<td>SSP Read Data</td>
</tr>
<tr>
<td>GPIO27/SSP1_EXTCLK</td>
<td>SSI_MCLK</td>
<td>SSP Master Clock</td>
</tr>
<tr>
<td>GPIO114</td>
<td>SSI_RDY</td>
<td>SSP Ready (or Interrupt)</td>
</tr>
<tr>
<td>GPIO19/SSP2_CLK</td>
<td>SPI0_CLK</td>
<td>SPI0 Clock</td>
</tr>
<tr>
<td>GPIO14/SSP2_FRM</td>
<td>*SPI0_CS0</td>
<td>SPI0 Chip Select</td>
</tr>
<tr>
<td>GPIO13/SSP2_TXD</td>
<td>SPI0_MOSI</td>
<td>SPI0 Master Out/Slave In</td>
</tr>
<tr>
<td>GPIO86/SSP2_RXD</td>
<td>SPI0_MISO</td>
<td>SPI0 Master In/Slave Out</td>
</tr>
<tr>
<td>GPIO22/SSP2_EXTCLK</td>
<td>SPI0_RDY</td>
<td>SPI0 Ready (or Interrupt)</td>
</tr>
<tr>
<td>GPIO84/SSP3_CLK</td>
<td>SPI1_CLK</td>
<td>SPI1 Clock</td>
</tr>
<tr>
<td>GPIO83/SSP3_FRM</td>
<td>*SPI1_CS0</td>
<td>SPI1 Chip Select</td>
</tr>
<tr>
<td>GPIO81/SSP3_TXD</td>
<td>SPI1_MOSI</td>
<td>SPI1 Master Out/Slave In</td>
</tr>
<tr>
<td>GPIO82/SSP3_RXD</td>
<td>SPI1_MISO</td>
<td>SPI1 Master In/Slave Out</td>
</tr>
</tbody>
</table>

Table 13 – PXA270 SSP/SPI Controllers to SODIMM Connections

5.7.1 PXA270 SSP/SPI INTERFACE NOTES

1. SODIMM SPI1 (PXA270 SSP3) is used off board to interface with the ADS7846 Touch Controller on the CSB702 “CSB7xx Base Board” or the optional CSB909xx LCD boards. This is the preferred use for this port.

2. SODIMM SPI0 (PXA270 SSP2) is routed to the I/O sites of the CSB902 “CSB7xx I/O Expansion board”.

3. SODIMM SSP (PXA270 SSP1) is routed to the SD/MMC Socket on the CSB902 “CSB7xx I/O Expansion board”. This port can then be used to control an SD/MMC card in 1-Bit SPI mode using PXA270 GPIO114 (SSP_RDY) as an optional ready or interrupt input.

4. Revision P4 of the CSB726 does not support the SODIMM SSI port
5.8 PXA270 I2C INTERFACE

The PXA270 has two I2C Interfaces. The first (via PXA270 GPIO117/I2C_SCL and GPIO118/I2C_SDA signals) is a full speed (100Khz/400Khz), master/slave I2C Serial Controller and is connected to the SODIMM I2C pins, I2C_SCL and I2C_SDA. The second (via PXA270 GPIO3/PWR_SCL and GPIO4/PWR_SDA signals) is a master only, lower speed (60/160Khz) interface and is used to control the ISL6271 core regulator. Refer to the PXA270 Users Manual for detailed programming information on both I2C Controllers.

The signals used to interface the PXA270 I2C controller to the SODIMM are shown in the following table.

<table>
<thead>
<tr>
<th>PXA270 Signal</th>
<th>SODIMM Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO117/I2C_SCL</td>
<td>I2C_SCL</td>
<td>I2C Bus Clock</td>
</tr>
<tr>
<td>GPIO118/I2C_SDA</td>
<td>I2C_SDA</td>
<td>I2C Bus Data</td>
</tr>
<tr>
<td>GPIO104</td>
<td>*I2C_INT</td>
<td>Shared I2C Bus Interrupt</td>
</tr>
</tbody>
</table>

Table 14 – PXA270 I2C Controller to SODIMM Connections

5.9 PXA270 4-BIT SD/MMC CONTROLLER

The PXA270 has a high-speed 4-Bit Secure Digital (SD/MMC) controller. This controller can interface with MMC, SD and SDIO Cards with minimal host intervention. The internal PXA270 DMA controller can be used to transfer data between the SD/MMC Socket on the target board and system memory for high data throughput (up to 80Mbits/sec in 4-bit mode). Refer to the PXA270 Users Manual for detailed programming information on the SD/MMC Controller.

The signals used to interface the PXA270 SD/MMC controller to the SODIMM are shown in the following table.

<table>
<thead>
<tr>
<th>PXA270 Signal</th>
<th>SODIMM Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO32/SD_CLK</td>
<td>SD0_CLK</td>
<td>SD Card Clock (SPI Mode Clock)</td>
</tr>
<tr>
<td>GPIO112/SD_CMD</td>
<td>SD0_DIN_CMD</td>
<td>SD Card Command (SPI Mode MISO)</td>
</tr>
<tr>
<td>GPIO92/SD_D0</td>
<td>SD0_DOUT_D0</td>
<td>SD Card Data 0 (SPI Mode MOSI)</td>
</tr>
<tr>
<td>GPIO109/SD_D1</td>
<td>SD0_IRQ_D1</td>
<td>SD Card Data 1 (SPI Mode IRQ)</td>
</tr>
</tbody>
</table>
5.10 PXA270 COMPACT FLASH INTERFACE

The PXA270 supports the Compact Flash Interface using the internal PCMCIA/CF Memory Controller. The CSB726 supports one socket via the SODIMM connector. Refer to the PXA270 Users Manual for detailed programming information on the Compact Flash Interface.

The signals used to interface with the Compact Flash are shown in the following table.

<table>
<thead>
<tr>
<th>PXA270 Signal</th>
<th>SODIMM Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO85/*PCE1</td>
<td>*CF_CE1</td>
<td>Chip Enable 1</td>
</tr>
<tr>
<td>GPIO54/*PCE2</td>
<td>*CF_CE2</td>
<td>Chip Enable 2</td>
</tr>
<tr>
<td>GPIO48/*PCOE</td>
<td>*CF_OE</td>
<td>Memory mode Output Enable</td>
</tr>
<tr>
<td>GPIO/*PCWE</td>
<td>*CF_WE</td>
<td>Memory mode Write Enable</td>
</tr>
<tr>
<td>GPIO/*PCIOR</td>
<td>*CF_IOR</td>
<td>I/O Mode Read Enable</td>
</tr>
<tr>
<td>GPIO/*PCIOW</td>
<td>*CF_IOW</td>
<td>I/O Mode Write Enable</td>
</tr>
<tr>
<td>PXA270 Signal</td>
<td>SODIMM Signal</td>
<td>Notes</td>
</tr>
<tr>
<td>---------------</td>
<td>---------------</td>
<td>-------</td>
</tr>
<tr>
<td>GPIO/*PCREG</td>
<td>*CF_REG</td>
<td>I/O Mode Enable</td>
</tr>
<tr>
<td>GPIO/*WAIT</td>
<td>*CF_WAIT</td>
<td>Wait signal to extend access time</td>
</tr>
<tr>
<td>GPIO98</td>
<td>CF_RDY</td>
<td>Ready (Memory mode), or Interrupt (I/O mode)</td>
</tr>
<tr>
<td>GPIO99</td>
<td>*CF_CD</td>
<td>Card Detect, 0 = Card Inserted</td>
</tr>
<tr>
<td>GPIO103</td>
<td>CF_RST</td>
<td>Card Reset (1= reset)</td>
</tr>
</tbody>
</table>

Table 16 – PXA270 to Compact Flash Connections

5.10.1 PXA270 COMPACT FLASH INTERFACE NOTES
1. The Data, Address and Control signals must be buffered on the target board before routing them to the Compact Flash socket.

2. The PXA270 provides *PSKTSEL (GPIO79) to select between two Compact Flash sockets. This is unused on the CSB726 as only one socket is supported.

3. The optional IOIS16 signal is not supported on the CSB726. GPIO57/*IOIS16 on the PXA270 should be assigned to GPIO (Alternate Function 0), output and set to 0.

4. Controlling power to the Compact Flash card is left to the target board designer. On the CSB902 “CSB7xx I/O Expansion Board” power to the Compact Flash Socket is enabled when *CF_CD = 0.

5.11 PXA270 USB HOST CONTROLLER
The PXA270 has two 12Mbit, USB 1.1 compliant Host Ports. The second Host Port is shared with the USB Device Port and must be configured appropriately. On the CSB726, USBH_P0 and USBH_N0 are routed to SODIMM signals USBH0_DP and USBH0_DM respectively, while USBH_P1 and USBH_N1 are routed to USBD_DP and USBD_DM.

5.11.1 PXA270 USB HOST INTERFACE NOTES
1. Power control for the external host port is left to the target board designer.

2. Over Current Indication is also left to the discretion of the target board designer.
5.12 **PXA270 USB DEVICE CONTROLLER**

The PXA270 has a single, 12Mbit, USB 1.1 compliant Device port (shared with USB Host Port 1). On the CSB726 USBH_P1 and USBH_N1 are routed to USBD_DP and USB_DM respectively. Refer to the PXA270 Users Manual for detailed programming information.

### 5.12.1 PXA270 USB DEVICE INTERFACE NOTES

1. The Cable Detect method if desired, is left to the target board designer. On the CSB702 “CSB7xx Base Board” an I2C GPIO expander is used to read the state of the USB Device Power pin. Refer to the CSB702 HW Reference Manual for more information.

2. The Soft Connect method if desired, is left to the target board designer. On the CSB702 “CSB7xx Base Board” an I2C GPIO expander is used to control Soft Connect. Refer to the CSB702 HW Reference Manual for more information.

5.13 **PXA270 AC97 AUDIO CODEC INTERFACE**

The PXA270 supports an external audio codec using the AC97 bus interface standard. On the CSB726 these signals are routed to the SODIMM AC97 Port.

The signals used to interface with the SODIMM AC97/I2S Port are shown in the following table.

<table>
<thead>
<tr>
<th>PXA270 Signal</th>
<th>SODIMM Signal</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO113/*AC97_RST</td>
<td>*AC_RST</td>
<td>AC97 Codec Reset</td>
</tr>
<tr>
<td>GPIO28/AC97_BCLK/I2S_BCLK</td>
<td>AC_BCLK</td>
<td>AC97 Codec Bit Clock</td>
</tr>
<tr>
<td>GPIO31/AC97_SYNC/I2S_SYNC</td>
<td>AC_SYNC</td>
<td>AC97 Frame Sync</td>
</tr>
<tr>
<td>GPIO30/AC97_SDOUT/I2S_SDOUT</td>
<td>AC_SDOUT</td>
<td>AC97 Serial Data Out</td>
</tr>
<tr>
<td>GPIO29/AC97_SDIN/I2S_SDIN</td>
<td>AC_RXD</td>
<td>AC97 Serial Data In</td>
</tr>
</tbody>
</table>

Table 17 – PXA270 AC97 Controller to SODIMM Connections

### 5.13.1 AC97 AUDIO INTERFACE NOTES

1. The PXA270 AC97 signals are multiplexed with the PXA270 I2S Controller. If desired these signals could be assigned to I2S use.
5.14 UNAVAILABLE PXA270 PERIPHERALS/SIGNALS

The following PXA270 peripherals/signals are not available on the CSB726. Note that GPIO usage, including unused GPIO, is shown in section 5.4.

<table>
<thead>
<tr>
<th>PXA270 Peripheral/Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>*VDD_FLT</td>
<td>Power Fault - Tied high to disable</td>
</tr>
<tr>
<td>*BAT_FLT</td>
<td>Battery Fault - Tied high to disable</td>
</tr>
<tr>
<td>SYSEN</td>
<td>Power Enable - Unconnected</td>
</tr>
<tr>
<td>16-Bit LCD I/F</td>
<td>LCD Interface – SM501 is used for LCD</td>
</tr>
<tr>
<td>10-Bit CIF I/F</td>
<td>Camera Interface – SM501 is used for Video Input.</td>
</tr>
<tr>
<td>KP_MKIN0-2</td>
<td>Matrix Keypad Input</td>
</tr>
<tr>
<td>KP_MKOUT0-4</td>
<td>Matrix Keypad Output</td>
</tr>
<tr>
<td>USIM I/F</td>
<td>Universal SIM Card Interface</td>
</tr>
<tr>
<td>MSL I/F</td>
<td>Mobile Scalable Link</td>
</tr>
<tr>
<td>MSHC I/F</td>
<td>Sony Memory Stick – Pins used for SD/MMC I/F</td>
</tr>
<tr>
<td>FIR</td>
<td>Fast Infrared – Pins used for RS232 debug port</td>
</tr>
<tr>
<td>PWM3</td>
<td>Used as SODIMM *PIRQ interrupt</td>
</tr>
</tbody>
</table>

Table 18 – PXA270 Unavailable Peripherals/Signals
6 CSB726 CLOCKING

6.1 PXA270 INPUT CLOCKS
The PXA270 is provided with two clocks. The first, 32.768Khz, is supplied from the DS1339 RTC. It is used by the PXA270 for its internal RTC as well as for power management and power sequencing. This clock must always be enabled from the DS1339.

The second clock is a 13Mhz crystal attached to the PXA270 PXTAL oscillator pins. This clock is used to drive the internal CPU and System PLL’s. The PXA270 core clock (520Mhz), as well as the SDRAM clock and Expansion Bus clock is derived from this clock.

6.2 PXA270 OUTPUT CLOCKS
The PXA270 drives two clocks that are used by the CSB726. The first is SDCLK0 and should be programmed for 52Mhz. This is used to drive the SODIMM signal EXP_CLK as well as the SM501 Host Bus Interface Clock (HCLK).

The second clock, SDCLK1 is used to drive the Mobile SDRAM and should be programmed to 104Mhz. Please refer to the PXA270 documentation for detailed clocking information.

A third clock, SDCLK2 is not used and should be disabled by SW to reduce power consumption and noise.

6.3 SM501 CLOCKS
The SM501 is supplied with a 52Mhz Bus interface clock on its HCLK pin. This clock is the reference clock for the host bus interface. The SM501 also has a 24Mhz crystal attached to its XTAL oscillator pins. This clock is the reference clock for the SM501 PLL’s and is used to derive all LCD output and Video Input Port Clocks as well as the internal frame buffer memory clock.

6.4 LAN9211 CLOCK
The LAN9211 has a 25Mhz crystal attached to its XTAL oscillator pins. It is used to derive all 10/100 Ethernet interface clocks.
7 CSB726 POWER MANAGEMENT

7.1 PXA270 PWR_EN (SODIMM *LOW_PWR)
The PXA270 outputs a signal called PWR_EN. When this signal is low, the PXA270 core regulator is disabled. The PXA270 PLL’s and I/O rails are still powered. This signal is used when the PXA270 is placed in “sleep to ram” mode. In this mode, the SDRAM devices are first placed in self-refresh mode, and then the PWR_EN signal is driven low. This signal is routed to the SODIMM *LOW_PWR pin. This allows external devices to be disabled if desired during “sleep to ram” mode. Refer to the PXA270 documentation for more detailed information about the PWR_EN signal.

7.2 PXA270 SYS_EN
This signal is driven by the PXA270 to shut down all power except the RTC rail. On the CSB726 this signal is not used. The SODIMM signal *PWR_DIS can be used to completely shut down the CSB726.

7.3 PXA270 BATTERY AND VDD FAULT
The PXA270 *BATT_FAULT and *VDD_FAULT signals are always driven high and are not used on the CSB726.

7.4 PXA270 CORE VOLTAGE
An Intersil ISL6271 device provides the .9V to 1.5V core voltage required by the PXA270. This device is controlled via I2C (PXA270 PWR_SCL and PWR_SDA), allowing SW to adjust the core voltage as required for a particular core frequency. This is known as “Dynamic Voltage/Frequency Scaling” or DVFS.

By default this regulator outputs 1.5V thus supporting the maximum 520Mhz PXA270 core frequency. Note that the ISL6271 output is disabled when PWR_EN is driven low by the PXA270. Refer to the PXA270 documentation for more detailed information about DVFS.

7.5 SODIMM *PWR_DIS
This signal can be driven low by external power management devices to disable the 3.3V-switching regulator. This will power the entire CSB726 down. Care must be taken to insure that the un-powered pins of the CSB726 devices will not interfere with other external devices that may be connected to those pins. Floating this signal (do not drive high) will enable the 3.3V-switching regulator.
8 CSB726 SOFTWARE

8.1 OVERVIEW
Due to the various resources contained on the CSB726, both on and off the PXA270, it is necessary to initialize a large number of PXA270 registers and external devices before correct operation can begin. These values and their proper sequencing are beyond the scope of this document. Contact Cogent for example boot initialization code.
9 SODIMM FORMAT AND PINOUT

9.1 OVERVIEW
This section defines the pinout of the SODIMM connector.

9.2 SODIMM FORMAT
The CSB726 is fully compatible with the Cogent CSB7xx family of SODIMM System On a Module (SOM) components. The SODIMM form factor is based on the JEDEC standard MO244 with 2.5V keying (note that this keying is not electrically significant for the CSB726, only for mechanical purposes). The only exceptions are the length of the module, 2.0" vs. 1.0" standard, and the presence of two .125" plated holes for mounting and power. Refer to the “CSB7xx R2 Design Guide” for detailed layout dimensions of the target board SODIMM socket and mounting-hole requirements.

9.3 SODIMM PINOUT
The CSB726 has a 200-pin SODIMM edge connector, with two sides, A and B. The following table describes the pinout of the connector. An "N" in the column marked CSB indicates that the signal is not supported by the CSB726.

In cases where the CSB7xx R2 SODIMM pinout defines multiple functions, the function used by the CSB726 is shown. For example, the PXA270 supports AC97 as opposed to I2S audio. Therefore the multi-function AC97/I2S port is labeled as AC97 for the CSB726.

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>CSB DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>DBG_TXD</td>
<td>DEBUG RS232 TRANSMIT</td>
</tr>
<tr>
<td>B1</td>
<td>DBG_RXD</td>
<td>DEBUG RS232 RECEIVE</td>
</tr>
<tr>
<td>A2</td>
<td>RTC_BAT</td>
<td>3V BATTERY INPUT TO DS1338 RTC</td>
</tr>
<tr>
<td>B2</td>
<td>*LOW_PWR</td>
<td>LOW POWER INDICATION FROM CPU</td>
</tr>
<tr>
<td>A3</td>
<td>*PWR_DIS</td>
<td>VCC3 DISABLE, 0 = OFF, FLOAT = ON</td>
</tr>
<tr>
<td>B3</td>
<td>*I2C_INT</td>
<td>I2C DEVICE INTERRUPT</td>
</tr>
<tr>
<td>A4</td>
<td>I2C_SCL</td>
<td>I2C BUS CLOCK</td>
</tr>
<tr>
<td>B4</td>
<td>I2C_SDA</td>
<td>I2C BUS DATA</td>
</tr>
<tr>
<td>A5</td>
<td>CPU_DBG0</td>
<td>N CPU SPECIFIC DEBUG SIGNAL</td>
</tr>
<tr>
<td>PIN</td>
<td>NAME</td>
<td>CSB</td>
</tr>
<tr>
<td>-----</td>
<td>------------</td>
<td>-----</td>
</tr>
<tr>
<td>B5</td>
<td>CPU_DBG1</td>
<td>N</td>
</tr>
<tr>
<td>A6</td>
<td>*CPU_TRST</td>
<td></td>
</tr>
<tr>
<td>B6</td>
<td>CPU_TMS</td>
<td></td>
</tr>
<tr>
<td>A7</td>
<td>CPU_TCK</td>
<td></td>
</tr>
<tr>
<td>B7</td>
<td>CPU_TDI</td>
<td></td>
</tr>
<tr>
<td>A8</td>
<td>CPU_TDO</td>
<td></td>
</tr>
<tr>
<td>B8</td>
<td>*RST_IN</td>
<td></td>
</tr>
<tr>
<td>A9</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B9</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A10</td>
<td>CAN0_TXD</td>
<td>N</td>
</tr>
<tr>
<td>B10</td>
<td>CAN0_RXD</td>
<td>N</td>
</tr>
<tr>
<td>A11</td>
<td>CAN1_TXD</td>
<td>N</td>
</tr>
<tr>
<td>B11</td>
<td>CAN1_RXD</td>
<td>N</td>
</tr>
<tr>
<td>A12</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B12</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A13</td>
<td>USBH0_P</td>
<td></td>
</tr>
<tr>
<td>B13</td>
<td>USBH1_P</td>
<td>N</td>
</tr>
<tr>
<td>A14</td>
<td>USBH0_N</td>
<td></td>
</tr>
<tr>
<td>B14</td>
<td>USBH1_N</td>
<td>N</td>
</tr>
<tr>
<td>A15</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B15</td>
<td>USBD_P</td>
<td></td>
</tr>
<tr>
<td>A16</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B16</td>
<td>USBD_N</td>
<td></td>
</tr>
<tr>
<td>A17</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B17</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A18</td>
<td>E_TD-</td>
<td></td>
</tr>
<tr>
<td>B18</td>
<td>E_RD-</td>
<td></td>
</tr>
<tr>
<td>A19</td>
<td>E_TD+</td>
<td></td>
</tr>
<tr>
<td>PIN</td>
<td>NAME</td>
<td>CSB DESCRIPTION</td>
</tr>
<tr>
<td>------</td>
<td>---------------</td>
<td>----------------------------------------</td>
</tr>
<tr>
<td>B19</td>
<td>E_RD+</td>
<td>ETHERNET RECEIVE DATA PLUS</td>
</tr>
<tr>
<td>A20</td>
<td>*E_LNK</td>
<td>ETHERNET LINK LED</td>
</tr>
<tr>
<td>B20</td>
<td>*E_SPD</td>
<td>ETHERNET SPEED LED</td>
</tr>
<tr>
<td>A21</td>
<td>*RST_OUT</td>
<td>SYSTEM RESET</td>
</tr>
<tr>
<td>B21</td>
<td>*TOUCH_INT</td>
<td>TOUCH SCREEN INTERRUPT</td>
</tr>
<tr>
<td>A22</td>
<td>GPIO0/IRQ0</td>
<td>GPIO0 (INTERRUPT VIA PXA270 GPIO1)</td>
</tr>
<tr>
<td>B22</td>
<td>GPIO1/IRQ1</td>
<td>GPIO1 (INTERRUPT VIA PXA270 GPIO11)</td>
</tr>
<tr>
<td>A23</td>
<td>GPIO2/TMR0</td>
<td>GPIO2 (TIMER VIA PXA270 GPIO9/CHOUT0)</td>
</tr>
<tr>
<td>B23</td>
<td>GPIO3/TMR1</td>
<td>GPIO3 (TIMER VIA PXA270 GPIO10/CHOUT1)</td>
</tr>
<tr>
<td>A24</td>
<td>GPIO4/PWM0</td>
<td>GPIO4 (PWM VIA PXA270 GPIO16/PWM0)</td>
</tr>
<tr>
<td>B24</td>
<td>GPIO5/PWM1</td>
<td>GPIO5 (PWM VIA PXA270 GPIO17/PWM1)</td>
</tr>
<tr>
<td>A25</td>
<td>GPIO6</td>
<td>GPIO BIT 6 (NO SPI 0 CHIP SELECT 1)</td>
</tr>
<tr>
<td>B25</td>
<td>GPIO7</td>
<td>GPIO BIT 7 (NO SPI 1 CHIP SELECT 1)</td>
</tr>
<tr>
<td>A26</td>
<td>GPIO8</td>
<td>GPIO BIT 8</td>
</tr>
<tr>
<td>B26</td>
<td>GPIO9</td>
<td>GPIO BIT 9</td>
</tr>
<tr>
<td>A27</td>
<td>SPI0_RDY/INT</td>
<td>SPI 0 READY OR INTERRUPT</td>
</tr>
<tr>
<td>B27</td>
<td>SPI0_MOSI</td>
<td>SPI 0 MASTER OUT/SLAVE IN</td>
</tr>
<tr>
<td>A28</td>
<td>SPI0_MISO</td>
<td>SPI 0 MASTER IN/SLAVE OUT</td>
</tr>
<tr>
<td>B28</td>
<td>*SPI0_CS0</td>
<td>SPI 0 CHIP SELECT 0</td>
</tr>
<tr>
<td>A29</td>
<td>SPI0_CLK</td>
<td>SPI 0 CLOCK</td>
</tr>
<tr>
<td>B29</td>
<td>SPI1_RDY/INT</td>
<td>N SPI 1 READY OR INTERRUPT</td>
</tr>
<tr>
<td>A30</td>
<td>SPI1_MOSI</td>
<td>SPI 1 MASTER OUT/SLAVE IN</td>
</tr>
<tr>
<td>B30</td>
<td>SPI1_MISO</td>
<td>SPI 1 MASTER IN/SLAVE OUT</td>
</tr>
<tr>
<td>A31</td>
<td>*SPI1_CS0</td>
<td>SPI 1 CHIP SELECT 0</td>
</tr>
<tr>
<td>B31</td>
<td>SPI1_CLK</td>
<td>SPI 1 CLOCK</td>
</tr>
<tr>
<td>A32</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B32</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A33</td>
<td>SD0_DOUT_D0</td>
<td>SD/MMC CARD 0 DATA 0</td>
</tr>
<tr>
<td>PIN</td>
<td>NAME</td>
<td>CSB DESCRIPTION</td>
</tr>
<tr>
<td>-----</td>
<td>-----------------</td>
<td>------------------------------------------------------</td>
</tr>
<tr>
<td>B33</td>
<td>SD0_IRQ_D1</td>
<td>SD/MMC CARD 0 DATA 1 (SDIO IRQ)</td>
</tr>
<tr>
<td>A34</td>
<td>SD0_D2</td>
<td>SD/MMC CARD 0 DATA 2</td>
</tr>
<tr>
<td>B34</td>
<td>SD0_CS_D3</td>
<td>SD/MMC CARD 0 DATA 3</td>
</tr>
<tr>
<td>A35</td>
<td>SD0_DIN_CMD</td>
<td>SD/MMC CARD 0 COMMAND</td>
</tr>
<tr>
<td>B35</td>
<td>SD0_CLK</td>
<td>SD/MMC CARD 0 CLOCK</td>
</tr>
<tr>
<td>A36</td>
<td>U0_TXD</td>
<td>UART 0 TRANSMIT</td>
</tr>
<tr>
<td>B36</td>
<td>U0_RXD</td>
<td>UART 0 RECEIVE</td>
</tr>
<tr>
<td>A37</td>
<td>U0_RTS</td>
<td>UART 0 REQUEST TO SEND</td>
</tr>
<tr>
<td>B37</td>
<td>U0_CTS</td>
<td>UART 0 CLEAR TO SEND</td>
</tr>
<tr>
<td>A38</td>
<td>U0_DTR</td>
<td>UART 0 DATA TERMINAL READY</td>
</tr>
<tr>
<td>B38</td>
<td>U0_DSR</td>
<td>UART 0 DATA SET READY</td>
</tr>
<tr>
<td>A39</td>
<td>U0_DCD</td>
<td>UART 0 DATA CARRIER DETECT</td>
</tr>
<tr>
<td>B39</td>
<td>U0_RI</td>
<td>UART 0 RING INDICATOR</td>
</tr>
<tr>
<td>A40</td>
<td>U1_TXD</td>
<td>UART 1 TRANSMIT</td>
</tr>
<tr>
<td>B40</td>
<td>U1_RXD</td>
<td>UART 1 RECEIVE</td>
</tr>
<tr>
<td>A41</td>
<td>U1_RTS</td>
<td>UART 1 REQUEST TO SEND</td>
</tr>
<tr>
<td>B41</td>
<td>U1_CTS</td>
<td>UART 1 CLEAR TO SEND</td>
</tr>
<tr>
<td>A42</td>
<td>AC_SDOUT</td>
<td>AC97 SERIAL DATA TO CODEC</td>
</tr>
<tr>
<td>B42</td>
<td>AC_SDIN</td>
<td>AC97 SERIAL DATA FROM CODEC</td>
</tr>
<tr>
<td>A43</td>
<td>AC_BCLK</td>
<td>AC97 BIT CLOCK FROM CODEC</td>
</tr>
<tr>
<td>B43</td>
<td>AC_SYNC</td>
<td>AC97 SYNC FROM CODEC</td>
</tr>
<tr>
<td>A44</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B44</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A45</td>
<td>*AC_RST</td>
<td>AC97 RESET TO CODEC</td>
</tr>
<tr>
<td>B45</td>
<td>SSI_RXD</td>
<td>SSI RECEIVE</td>
</tr>
<tr>
<td>A46</td>
<td>SSI_RDY</td>
<td>SSI READY</td>
</tr>
<tr>
<td>B46</td>
<td>SSI_MCLK</td>
<td>SSI MASTER CLOCK</td>
</tr>
<tr>
<td>A47</td>
<td>SSI_FRM</td>
<td>SSI FRAME</td>
</tr>
<tr>
<td>PIN</td>
<td>NAME</td>
<td>CSB DESCRIPTION</td>
</tr>
<tr>
<td>-----</td>
<td>------------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>B47</td>
<td>SSI_TXD</td>
<td>SSI TRANSMIT</td>
</tr>
<tr>
<td>A48</td>
<td>SS1_CLK</td>
<td>SSI MASTER CLOCK</td>
</tr>
<tr>
<td>B48</td>
<td>*CF_CE1</td>
<td>COMPACT FLASH CHIP ENABLE 1</td>
</tr>
<tr>
<td>A49</td>
<td>*CF_CE2</td>
<td>COMPACT FLASH CHIP ENABLE 2</td>
</tr>
<tr>
<td>B49</td>
<td>*CF_REG</td>
<td>COMPACT FLASH I/O REGISTER SPACE</td>
</tr>
<tr>
<td>A50</td>
<td>*CF_OE</td>
<td>COMPACT FLASH MEMORY OUTPUT ENABLE</td>
</tr>
<tr>
<td>B50</td>
<td>*CF_WE</td>
<td>COMPACT FLASH MEMORY WRITE ENABLE</td>
</tr>
<tr>
<td>A51</td>
<td>*CF_IOR</td>
<td>COMPACT FLASH I/O READ STROBE</td>
</tr>
<tr>
<td>B51</td>
<td>*CF_IOW</td>
<td>COMPACT FLASH I/O WRITE STROBE</td>
</tr>
<tr>
<td>A52</td>
<td>*CF_WAIT</td>
<td>COMPACT FLASH WAIT</td>
</tr>
<tr>
<td>B52</td>
<td>CF_RDY</td>
<td>COMPACT FLASH READY/BUSY/INTERRUPT</td>
</tr>
<tr>
<td>A53</td>
<td>CF_RST</td>
<td>COMPACT FLASH RESET</td>
</tr>
<tr>
<td>B53</td>
<td>*CF_CD</td>
<td>COMPACT FLASH CARD DETECT</td>
</tr>
<tr>
<td>A54</td>
<td>*EXP_CS</td>
<td>EXPANSION CHIP SELECT</td>
</tr>
<tr>
<td>B54</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A55</td>
<td>EXP_CLK</td>
<td>EXPANSION BUS CLOCK</td>
</tr>
<tr>
<td>B55</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A56</td>
<td>*EXP_WAIT</td>
<td>EXPANSION WAIT</td>
</tr>
<tr>
<td>B56</td>
<td>*EXP_IRQ</td>
<td>EXPANSION INTERRUPT</td>
</tr>
<tr>
<td>A57</td>
<td>*EXP_WE</td>
<td>EXPANSION WRITE ENABLE</td>
</tr>
<tr>
<td>B57</td>
<td>*EXP_OE</td>
<td>EXPANSION READ ENABLE</td>
</tr>
<tr>
<td>A58</td>
<td>*EXP_BE0</td>
<td>EXPANSION BYTE ENABLE 0</td>
</tr>
<tr>
<td>B58</td>
<td>*EXP_BE1</td>
<td>EXPANSION BYTE ENABLE 1</td>
</tr>
<tr>
<td>A59</td>
<td>LD0</td>
<td>COMPACT FLASH/EXPANSION DATA BIT0</td>
</tr>
<tr>
<td>B59</td>
<td>LD1</td>
<td>COMPACT FLASH/EXPANSION DATA BIT1</td>
</tr>
<tr>
<td>A60</td>
<td>LD2</td>
<td>COMPACT FLASH/EXPANSION DATA BIT2</td>
</tr>
<tr>
<td>B60</td>
<td>LD3</td>
<td>COMPACT FLASH/EXPANSION DATA BIT3</td>
</tr>
<tr>
<td>A61</td>
<td>LD4</td>
<td>COMPACT FLASH/EXPANSION DATA BIT4</td>
</tr>
<tr>
<td>PIN</td>
<td>NAME</td>
<td>CSB DESCRIPTION</td>
</tr>
<tr>
<td>-----</td>
<td>------</td>
<td>-----------------</td>
</tr>
<tr>
<td>B61</td>
<td>LD5</td>
<td>COMPACT FLASH/EXPANSION DATA BIT5</td>
</tr>
<tr>
<td>A62</td>
<td>LD6</td>
<td>COMPACT FLASH/EXPANSION DATA BIT6</td>
</tr>
<tr>
<td>B62</td>
<td>LD7</td>
<td>COMPACT FLASH/EXPANSION DATA BIT7</td>
</tr>
<tr>
<td>A63</td>
<td>LD8</td>
<td>COMPACT FLASH/EXPANSION DATA BIT8</td>
</tr>
<tr>
<td>B63</td>
<td>LD9</td>
<td>COMPACT FLASH/EXPANSION DATA BIT9</td>
</tr>
<tr>
<td>A64</td>
<td>LD10</td>
<td>COMPACT FLASH/EXPANSION DATA BIT10</td>
</tr>
<tr>
<td>B64</td>
<td>LD11</td>
<td>COMPACT FLASH/EXPANSION DATA BIT11</td>
</tr>
<tr>
<td>A65</td>
<td>LD12</td>
<td>COMPACT FLASH/EXPANSION DATA BIT12</td>
</tr>
<tr>
<td>B65</td>
<td>LD13</td>
<td>COMPACT FLASH/EXPANSION DATA BIT13</td>
</tr>
<tr>
<td>A66</td>
<td>LD14</td>
<td>COMPACT FLASH/EXPANSION DATA BIT14</td>
</tr>
<tr>
<td>B66</td>
<td>LD15</td>
<td>COMPACT FLASH/EXPANSION DATA BIT15</td>
</tr>
<tr>
<td>A67</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B67</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A68</td>
<td>LA0</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 0</td>
</tr>
<tr>
<td>B68</td>
<td>LA1</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 1</td>
</tr>
<tr>
<td>A69</td>
<td>LA2</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 2</td>
</tr>
<tr>
<td>B69</td>
<td>LA3</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 3</td>
</tr>
<tr>
<td>A70</td>
<td>LA4</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 4</td>
</tr>
<tr>
<td>B70</td>
<td>LA5</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 5</td>
</tr>
<tr>
<td>A71</td>
<td>LA6</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 6</td>
</tr>
<tr>
<td>B71</td>
<td>LA7</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 7</td>
</tr>
<tr>
<td>A72</td>
<td>LA8</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 8</td>
</tr>
<tr>
<td>B72</td>
<td>LA9</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 9</td>
</tr>
<tr>
<td>A73</td>
<td>LA10</td>
<td>COMPACT FLASH/EXPANSION ADDRESS BIT 10</td>
</tr>
<tr>
<td>B73</td>
<td>LA11</td>
<td>EXPANSION ADDRESS BIT 11</td>
</tr>
<tr>
<td>A74</td>
<td>LA12</td>
<td>EXPANSION ADDRESS BIT 12</td>
</tr>
<tr>
<td>B74</td>
<td>LA13</td>
<td>EXPANSION ADDRESS BIT 13</td>
</tr>
<tr>
<td>A75</td>
<td>LA14</td>
<td>EXPANSION ADDRESS BIT 14</td>
</tr>
<tr>
<td>PIN</td>
<td>NAME</td>
<td>CSB DESCRIPTION</td>
</tr>
<tr>
<td>-----</td>
<td>------</td>
<td>-----------------</td>
</tr>
<tr>
<td>B75</td>
<td>LA15</td>
<td>EXPANSION ADDRESS BIT 15</td>
</tr>
<tr>
<td>A76</td>
<td>LA16</td>
<td>EXPANSION ADDRESS BIT 16</td>
</tr>
<tr>
<td>B76</td>
<td>LA17</td>
<td>EXPANSION ADDRESS BIT 17</td>
</tr>
<tr>
<td>A77</td>
<td>LA18</td>
<td>EXPANSION ADDRESS BIT 18</td>
</tr>
<tr>
<td>B77</td>
<td>LA19</td>
<td>EXPANSION ADDRESS BIT 19</td>
</tr>
<tr>
<td>A78</td>
<td>LA20</td>
<td>EXPANSION ADDRESS BIT 20</td>
</tr>
<tr>
<td>B78</td>
<td>LA21</td>
<td>EXPANSION ADDRESS BIT 21</td>
</tr>
<tr>
<td>A79</td>
<td>LA22</td>
<td>EXPANSION ADDRESS BIT 22</td>
</tr>
<tr>
<td>B79</td>
<td>LA23</td>
<td>EXPANSION ADDRESS BIT 23</td>
</tr>
<tr>
<td>A80</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B80</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A81</td>
<td>LA24</td>
<td>EXPANSION ADDRESS BIT 24</td>
</tr>
<tr>
<td>B81</td>
<td>LCD_B0</td>
<td>LCD BLUE BIT 0</td>
</tr>
<tr>
<td>A82</td>
<td>LCD_B1</td>
<td>LCD BLUE BIT 1</td>
</tr>
<tr>
<td>B82</td>
<td>LCD_B2</td>
<td>LCD BLUE BIT 2</td>
</tr>
<tr>
<td>A83</td>
<td>LCD_B3</td>
<td>LCD BLUE BIT 3</td>
</tr>
<tr>
<td>B83</td>
<td>LCD_B4</td>
<td>LCD BLUE BIT 4</td>
</tr>
<tr>
<td>A84</td>
<td>LCD_B5</td>
<td>LCD BLUE BIT 5</td>
</tr>
<tr>
<td>B84</td>
<td>LCD_G0</td>
<td>LCD GREEN BIT 0</td>
</tr>
<tr>
<td>A85</td>
<td>LCD_G1</td>
<td>LCD GREEN BIT 1</td>
</tr>
<tr>
<td>B85</td>
<td>LCD_G2</td>
<td>LCD GREEN BIT 2</td>
</tr>
<tr>
<td>A86</td>
<td>LCD_G3</td>
<td>LCD GREEN BIT 3</td>
</tr>
<tr>
<td>B86</td>
<td>LCD_G4</td>
<td>LCD GREEN BIT 4</td>
</tr>
<tr>
<td>A87</td>
<td>LCD_G5</td>
<td>LCD GREEN BIT 5</td>
</tr>
<tr>
<td>B87</td>
<td>LCD_R0</td>
<td>LCD RED BIT 0</td>
</tr>
<tr>
<td>A88</td>
<td>LCD_R1</td>
<td>LCD RED BIT 1</td>
</tr>
<tr>
<td>B88</td>
<td>LCD_R2</td>
<td>LCD RED BIT 2</td>
</tr>
<tr>
<td>A89</td>
<td>LCD_R3</td>
<td>LCD RED BIT 3</td>
</tr>
<tr>
<td>PIN</td>
<td>NAME</td>
<td>CSB DESCRIPTION</td>
</tr>
<tr>
<td>------</td>
<td>------------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>B89</td>
<td>LCD_R4</td>
<td>LCD RED BIT 4</td>
</tr>
<tr>
<td>A90</td>
<td>LCD_R5</td>
<td>LCD RED BIT 5</td>
</tr>
<tr>
<td>B90</td>
<td>LCD_HSYNC</td>
<td>LCD HORIZONTAL SYNC</td>
</tr>
<tr>
<td>A91</td>
<td>LCD_VSYNC</td>
<td>LCD VERTICAL SYNC</td>
</tr>
<tr>
<td>B91</td>
<td>LCD_OE</td>
<td>LCD OUTPUT ENABLE</td>
</tr>
<tr>
<td>A92</td>
<td>LCD_PCLK</td>
<td>LCD PIXEL CLOCK</td>
</tr>
<tr>
<td>B92</td>
<td>LCD_BKL</td>
<td>LCD BACKLIGHT ENABLE</td>
</tr>
<tr>
<td>A93</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>B93</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>A94</td>
<td>VIP_MCLK</td>
<td>N  MASTER CLOCK OUT TO VIP DEVICE</td>
</tr>
<tr>
<td>B94</td>
<td>VIP_PCLK</td>
<td>VIDEO INPUT PORT PIXEL CLOCK</td>
</tr>
<tr>
<td>A95</td>
<td>VIP_HSYNC</td>
<td>VIDEO INPUT PORT HORIZONTAL SYNC</td>
</tr>
<tr>
<td>B95</td>
<td>VIP_VSYNC</td>
<td>VIDEO INPUT PORT VERTICAL SYNC</td>
</tr>
<tr>
<td>A96</td>
<td>VIP_D0</td>
<td>VIDEO INPUT PORT BIT 0</td>
</tr>
<tr>
<td>B96</td>
<td>VIP_D1</td>
<td>VIDEO INPUT PORT BIT 1</td>
</tr>
<tr>
<td>A97</td>
<td>VIP_D2</td>
<td>VIDEO INPUT PORT BIT 2</td>
</tr>
<tr>
<td>B97</td>
<td>VIP_D3</td>
<td>VIDEO INPUT PORT BIT 3</td>
</tr>
<tr>
<td>A98</td>
<td>VIP_D4</td>
<td>VIDEO INPUT PORT BIT 4</td>
</tr>
<tr>
<td>B98</td>
<td>VIP_D5</td>
<td>VIDEO INPUT PORT BIT 5</td>
</tr>
<tr>
<td>A99</td>
<td>VIP_D6</td>
<td>VIDEO INPUT PORT BIT 6</td>
</tr>
<tr>
<td>B99</td>
<td>VIP_D7</td>
<td>VIDEO INPUT PORT BIT 7</td>
</tr>
<tr>
<td>A100</td>
<td>VIP_D8</td>
<td>N  VIDEO INPUT PORT BIT 8 (10-BIT MODE ONLY)</td>
</tr>
<tr>
<td>B100</td>
<td>VIP_D9</td>
<td>N  VIDEO INPUT PORT BIT 9 (10-BIT MODE ONLY)</td>
</tr>
</tbody>
</table>

Table 19 – CSB726 SODIMM Expansion Connector Pinout
10 COMPONENT LOCATIONS

10.1 OVERVIEW
The following figure shows the component locations for the CSB726 Top and Bottom sides. These are shown for reference purposes only.

Figure 2 – CSB726 Component Locations
### 11 DOCUMENT REVISIONS

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>12/1/2007</td>
<td>P4.0</td>
<td>First Release for SODIMM Pinout R1</td>
</tr>
</tbody>
</table>

Table 20 – Document Revisions