Intelligent Tools for
Extended JTAG/Boundary Scan

SCANFLEX
VARIOCORE

New

Intelligent Boundary Scan Solutions®
Why JTAG/Boundary Scan?

The requirement to test electronic components is as old as the electronics industry itself. While functional test has been used in the early days, in the 1970s the era of In-Circuit-test (ICT) began. ICT is based on mechanical access to test points on the printed circuit board (PCB) through so-called bed-of-nail adapters, providing the means of accessing the Unit Under Test and dividing it into individually testable partitions (structured test). This extraordinary test technology dominated the testing of electronics worldwide for many years, continuously improving, until one problem became impossible to solve – continuously reduced test access. Ever decreasing mechanical test access is the result of more and more complex board structures and the use of space saving package technologies such as BGA (Ball Grid Array), microBGA and CSP (Chip Scale Package). A new test technology named Boundary Scan (also known as JTAG) had been developed, and finally standardized as IEEE-Std. 1149.1 in 1990. JTAG/Boundary Scan is a test access methodology as revolutionary as ICT was in its time. It offers the advantage of structural device, board and system level test access throughout the whole product life cycle without the need for any invasive nail access. JTAG/Boundary Scan guarantees reduced test costs and provides better test coverage. In addition to subset .1, JTAG/Boundary Scan meanwhile includes the standards IEEE 1149.4 (analog) and IEEE 1149.6 (Advanced Digital Networks).

GÖPEL electronic is one of the pioneers in JTAG/Boundary Scan applications and a worldwide leading vendor of comprehensive software and hardware tool sets, offering Intelligent Solutions for Extended JTAG/Boundary Scan.

GÖPEL electronic GmbH was established in Jena, Germany, in 1991, and over the years opened branch offices in Europe and the United States of America. Before starting GÖPEL electronic, its founding members were working on test technologies for integrated circuits at Carl-Zeiss Jena, Germany. GÖPEL was the first European supplier of software and hardware solutions for JTAG/Boundary Scan applications. Being a technology driver from the very beginning, CASCON GALAXY®, the first fully integrated software environment for JTAG/Boundary Scan application development, and the first IEEE 1149.1 controller card for PXI are only two among many firsts introduced by GÖPEL electronic. Our philosophy of developing “intelligent tools” differentiates us from other vendors and allows us to support Extended JTAG/Boundary Scan applications.

Due to our worldwide presence, our extraordinary service and customer support commitment, and the design of our products to customer requirements, we are the favoured supplier in many industries such as telecommunication, Automotive and EMS. GÖPEL electronic is an ISO 9001 certified company since 1996. Highest customer satisfaction and product quality are our ultimate goal.
What is JTAG/Boundary Scan?

JTAG/Boundary Scan is possibly the most resourceful test access technique around. Similar to In-Circuit Test (ICT), but without physical bed-of-nail adapters, it detects structural fault locations by utilizing thousands of test points—with only four test bus lines. JTAG/Boundary Scan essentially means “testing at the periphery (boundaries) of a circuit.” In addition to the core logic and the “test points” (JTAG/Boundary Scan cells), an IEEE 1149.1 compliant IC (Integrated Circuit) also features some test scan cells, serving as test points to access the signals included in a specific test, are integrated between the core logic and the physical pins of the IC. This IC level test access architecture and the test bus connections between IEEE 1149.1 compliant devices are necessary for the use of JTAG/Boundary Scan. With those resources it is possible to:
- test particular components (device test)
- test the connection between I/O pins on the PCB and even between multiple PCBs
- test the function of complete boards under operating conditions as well as in stress test environments

Not all components on the board have to be JTAG/Boundary Scan compliant devices to achieve good test coverage. Even if only one component meets the requirement, JTAG/Boundary Scan can be used for certain test applications. Unlike other test access methodologies, JTAG/Boundary Scan can be utilized from the beginning to the end of a product life cycle for the following applications:
- design validation
- prototype verification
- device, board and system level test
- in-system programming

Please ask us to run a testability analysis on your boards to show you the test access available and discuss possible JTAG/Boundary Scan applications on your design. For details please refer to the JTAG/Boundary Scan software section on www.goepel.com.

JTAG/Boundary Scan has many advantages and enormous cost savings potential:

Benefits
- usable throughout the entire product life cycle
- no bed-of-nails fixture necessary—nevertheless offering very high test and fault coverage
- accelerates development of new products ➔ reduced Time-to-Market
- accelerates development of new products ➔ fast turnaround, e.g. for design changes
- improved product quality by combining testing and “just-in-time” on-board/in-system programming on production floor

Cost savings:
- low initial investment and cost of maintenance compared to other test technologies
- no storage costs, e.g. for test fixtures or pre-programmed devices
- fast amortisation ➔ high Return-On-Investment

Do not hesitate to ask us for a customised cost savings plan by utilising JTAG/Boundary Scan for your test applications in respect to your individual production volume. You can find further information on our website www.goepel.com.
The quality of a JTAG/Boundary Scan systems is primarily defined by the performance and the architecture of its software. In 1991, Göpel electronic was the worldwide first vendor to introduce a specialised software technology in form of an Integrated JTAG/Boundary Scan Development Environment (IDE) - SYSTEM CASCON™ was born. The uniqueness of this JTAG/Boundary Scan Workbench has been maintained over the years through continuous integration of new, intelligent tools paired with innovative system extensions and improvements in the user interface.

Today, SYSTEM CASCON™ is available in its fourth generation and is the only JTAG/Boundary Scan software that can claim the status of an open, graphical JTAG/Boundary Scan operating system. Its architecture thoroughly implements Göpel electronic’s philosophy of extended JTAG/Boundary Scan, eclipsing other solutions in regard of test coverage and system functionality by combining various tests, programming and emulation methods with native JTAG/Boundary Scan procedures. More than 4,500 systems delivered attest for the market leading position of SYSTEM CASCON™.

**Six intelligent reasons for SYSTEM CASCON™**

- Intelligent Data Base – to manage non-Boundary Scan structures
- Intelligent Programming Language – for unlimited flexibility
- Intelligent Tools – for excellent fault coverage with the push of a button
- Intelligent Protection – for highest performance with safe vectors
- Intelligent Fault Diagnostic – for precise and systematic fault localisation
- Intelligent User Interface – for team work and rapid project development

**JTAG/Boundary Scan Software with intelligence**

**SYSTEM CASCON™ architecture**

**Test Program (TP) Development Toolsuite**
- ATEPG Flying (Guided) Probe
- ATEPG Logic Components
- ATEPG Memory Access
- ATEPG Device Cluster
- ATEPG Interconnection 1149.6
- ATEPG Interconnection 1149.1
- ATEPG Infrastructure
- Universal Manual TP Generation
- TP Generation 1149.4

**Pin Fault Diagnostics (PFD) Toolsuite**
- PFD Flying (Guided) Probe
- PFD Logic Components
- PFD Memory Access
- PFD Device Cluster
- PFD Interconnection 1149.6
- PFD Interconnection 1149.1
- PFD Infrastructure
- Universal Pin Failure Detection
- Failure diagnostics 1149.4

**In-System Programming (ISP) Development Toolsuite**
- Automatic Flash Device ISP
- Manual Flash Device ISP
- PLD Program Generators
  - IEEE1532 / SVF / JAM / STAPL
- Data Import Processors
  - TDS / TBC / SVF / JAM / STAPL
- Data Export Processors
  - TDS / TBC / SVF / JAM / STAPL

**Data Merging, Browsing and Analysis Toolsuite**
- Design and Testability Explorer
- DFT Design Rule Checker
- Netlist Merger
- Test Coverage Analyzer
- Scan Vision Schematic
- Scan Vision Layout
- Multi Mode Debugger
- Advanced Vector Browser

**System Administration and System Control Modules**

**Application Execution and Flow Control Modules**
One software for all applications

The completely integrated architecture of SYSTEM CASCON™ provides the flexibility needed to adapt the software configuration to completely different target applications and environments. In this regard, so-called Enable Codes are used as keys to activate or deactivate specific tools and modules of the system. For the user this approach provides enormous benefits over multi-package solutions since the software configuration can be changed easily and quickly. The handling of updates and upgrades is extremely simple, and problems due to incompatible tools are prevented. Software packages designed for laboratory, production, and field service are available in various performance classes (Editions) as Development Stations (DS) and Test/Execution Stations (TS/ES). Pure in-system Programming (ISP) applications can be realised with CASCON POLARIS™ Editions, while CASCON GALAXY® supports both ISP and test procedures. The extensive CASCON Application Programming Interface (CAPI) enables powerful integrations. Floating Licenses provide extreme efficiency with Multi-Seat and Multi-Tooling capabilities.

### CASCON GALAXY® configuration matrix

<table>
<thead>
<tr>
<th>Available Tools and Modules</th>
<th>CASCON GALAXY® Development Stations (DS)</th>
<th>CASCON GALAXY® Test Stations (TS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATPG Flying (Guided) Probe</td>
<td>option</td>
<td>option</td>
</tr>
<tr>
<td>ATPG Logic Components</td>
<td>option</td>
<td>option</td>
</tr>
<tr>
<td>ATPG Memory Access</td>
<td>option</td>
<td>option</td>
</tr>
<tr>
<td>ATPG Device Cluster</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>ATPG Interconnection 1149.6</td>
<td>option</td>
<td>option</td>
</tr>
<tr>
<td>ATPG Interconnection 1149.1</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>ATPG Infrastructure</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Universal Manual TP Generation</td>
<td>Universal Pin Failure Detection</td>
<td>✓</td>
</tr>
<tr>
<td>TP Generation 1149.4</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Design and Testability Explorer</td>
<td>Automatic Flash Device ISP</td>
<td>✓</td>
</tr>
<tr>
<td>DfT Design Rule Checker</td>
<td>Manual Flash Device ISP</td>
<td>option</td>
</tr>
<tr>
<td>Netlist Merger</td>
<td>PLD Program Generators IEEE1532 / SVF / JAM / STAPL</td>
<td>option</td>
</tr>
<tr>
<td>Test Coverage Analyzer</td>
<td>TDS / TBO / SVF / JAM / STAPЛ</td>
<td>option</td>
</tr>
<tr>
<td>Scan Vision Schematic</td>
<td>Data Import Processors</td>
<td>option</td>
</tr>
<tr>
<td>Scan Vision Layout</td>
<td>TDS / TBO / SVF / JAM / STAPЛ</td>
<td>option</td>
</tr>
<tr>
<td>Multi Mode Debugger</td>
<td>Data Export Processors</td>
<td>option</td>
</tr>
<tr>
<td>Advanced Vector Browser</td>
<td>TDS / TBO / SVF / JAM / STAPЛ</td>
<td>✓</td>
</tr>
<tr>
<td>CASCON Full Platform License</td>
<td>Test / ISP / Batch Execution Modules</td>
<td>✓</td>
</tr>
<tr>
<td>CASCON API (CAPI)</td>
<td>VarioCore™ Handler</td>
<td>✓</td>
</tr>
<tr>
<td>Multi User Manager (myCASCON)</td>
<td>Hybrid Vector Splitter (HYSCAN)</td>
<td>✓</td>
</tr>
<tr>
<td>Floating License Module Manager</td>
<td>System Level Scan Router Handler</td>
<td>✓</td>
</tr>
<tr>
<td>Automated Process Scripting</td>
<td>Gang Test / Gang ISP Handler</td>
<td>✓</td>
</tr>
</tbody>
</table>
Choosing the right Edition

While the selection of the right CASCON POLARIS™ Edition is fairly simple, CASCON GALAXY® Development Stations provide a wide variety of features to choose from. The extraordinary modularity of this software package calls for careful consideration when deciding which edition, possibly supplemented by various options, to choose. The requirements on the software capabilities increase with a growing complexity of the Unit Under Test (UUT) and with the increasing number of projects. In particular, the productivity of automated tools for test pattern generation (ATPG) and pin-level fault diagnostics (PFD) are important in this regard. Increasing complexity of future projects should be taken into account as well when selecting which software to purchase. Software modules for system administration and Application Execution Modules are included in every SYSTEM CASCON™ Edition. With CASCON POLARIS™, the ISP Execution Modules are partially limited (depending on the edition) and the only test type supported is the Infrastructure Test. The ability to simply and quickly upgrade SYSTEM CASCON™ packages allows the initial investment to be kept as small as necessary. Even POLARIS packages can be upgraded to GALAXY packages at any time. Short term requirements can be satisfied with temporary activation of specific tools or complete editions.

CASCON POLARIS™ configuration matrix

<table>
<thead>
<tr>
<th>Available System Tools and Modules</th>
<th>CASCON POLARIS™ Editions</th>
<th>CASCON POLARIS™ Development Station (DS)</th>
<th>CASCON POLARIS™ Execution Station (ES)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATPG Infrastructure</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Design Explorer</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Manual Flash Device ISP</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PLD Program Generators</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Data Import Processors</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Data Export Processors</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CASCON ISP Platform License</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CASCON API (CAPI)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Multi User Manager (myCASCON)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Floating License Module Manager</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Automated Process Scripting</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

Choosing the right Edition

Project Inspector

The multiphase Project Inspector provides a consistent Graphical User Interface in SYSTEM CASCON™ for all tasks required for a JTAG/Boundary Scan project, including the generation of an intelligent UUT data base, the development of all JTAG/Boundary Scan Test and ISP procedures, and the project data analysis and verification. The Project Inspector provides context sensitive access to all development, execution and diagnostic tools as well as to all input and output files, including test coverage reports.

<table>
<thead>
<tr>
<th>Number of designs or test applications to be supported</th>
<th>GALAXY Classic Edition with options</th>
<th>GALAXY Advanced Edition with options</th>
<th>GALAXY Advanced Edition with options</th>
</tr>
</thead>
<tbody>
<tr>
<td>low</td>
<td>low</td>
<td>medium</td>
<td>high</td>
</tr>
<tr>
<td></td>
<td>Complexity / Intelligence of the Unit Under Test (UUT)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Run Time with Advanced Vector Browser**
A quick overview of the applied test vectors with detected faults highlighted is available with the Advanced Vector Browser (AVB), in addition to plain text diagnostic messages in the test execution report. The pin and net level information in the AVB is scalable to allow an overview or in-depth investigation into individual pins and nets. The layout of the report file can be customised using the Report/Log File Generator to adjust the output to match a specific format.

**Debugger**
SYSTEM CASCON’s Multi Mode Debugger supports both interpretative executions of CASLAN programs as well as interactive debugging. A comprehensive tool set – including, but not limited to, Watch, Break, and Trace functions – provides visibility to JTAG/Boundary Scan logic and functional states. Test programs can easily be verified and test patterns can be modified at run-time. Both manually written and automatically generated test programs can be debugged.

**Graphical Library**
The graphical Device Library supports both JTAG/Boundary Scan ICs and non-Boundary Scan components (that have functional descriptions such as FLASH, RAM, Buffer, and other devices). BSDL files can be imported and exported. A graphical editor allows for interactive device model creation. A system library is included in the standard package.

**Scan Vision**
Scan Vision is an interactive JTAG/Boundary Scan Visualizer for Schematic and Layout, providing Cross-Probing capability and access to a graphical representation of UUT features from various SYSTEM CASCON™ tools such as the Net List Browser, Test Coverage Analyzer, Pin Fault Diagnostics or the Debugger. Different types of nets and logic levels on pins can be highlighted in various colours as defined by the user. To utilise Scan Vision, optional CAD Reader for schematic and layout are required.
JTAG/Boundary Scan Hardware with extraordinary features

Even the best JTAG/Boundary Scan software is not efficient if the applied hardware is missing important features and performance. Göpel electronic offers the widest spectrum of hardware solutions. The new SCANFLEX® hardware is by far the most innovative system architecture available on the market. SCANFLEX® is the only JTAG/Boundary Scan hardware platform that fully implements the philosophy of Extended JTAG/Boundary Scan in a modular, open and scalable environment. SCANFLEX® is a perfect fit for mid range and high-end performance applications. This hardware platform is complemented by ScanBooster™ JTAG/Boundary Scan controllers offering mid range performance for the low cost segment. This variety allows the right hardware to be selected to match the BScan application, throughput requirements and target environment.

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**System architecture overview**

**SCANFLEX® components**
- Controller
  - TAP Transceiver
  - TAP Interface Card (TIC)
  - I/O Modules

**SCANFLEX® additional resources**
- TAP Transceiver Auxiliary I/O
- Generic Digital I/O Module
- Generic Analog I/O Module
- Customised I/O Module
- VarioCore® I/O Module

**Supported Standards**
- IEEE 1149.1
- IEEE 1149.4
- IEEE 1149.6
- IEEE 1532
- JESD 71

**Related future standards**

**Applications**
- Extended Tests
- Extended Verification
- Concurrent PLD Programming
- High Speed Flash Programming

### SCANFLEX®/ Scan Booster™ Controller

<table>
<thead>
<tr>
<th>Controller Type</th>
<th>Bus Platform</th>
<th>Scan Architecture</th>
<th>TCK max</th>
<th>TAP</th>
<th>TAP Transceiver</th>
<th>HYSCAN™</th>
<th>ADYCS™ II</th>
<th>FASTSCALE™</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFX/xxx1149-C</td>
<td>PCI, PXI, VXI, USB2.0</td>
<td>SPACE™ II-5 Chipset</td>
<td>80 MHz</td>
<td>1 to 8</td>
<td>External</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SFX/xxx1149-B</td>
<td>PCI, PXI, VXI, USB2.0, LAN10/100, FireWire</td>
<td>SPACE™ II Chipset</td>
<td>50 MHz</td>
<td>1 to 8</td>
<td>External</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>SFX/xxx1149-A</td>
<td>PXI, USB2.0, PCIe</td>
<td>Data Buffer</td>
<td>20 MHz</td>
<td>1 to 8</td>
<td>External</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>Scan Booster/xxx</td>
<td>PCI, PXI, USB2.0</td>
<td>Data Buffer</td>
<td>16 MHz</td>
<td>1 to 2</td>
<td>On-Board</td>
<td>☀</td>
<td>☀</td>
<td>☀</td>
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</tbody>
</table>
SCANFLEX® TAP Transceiver

<table>
<thead>
<tr>
<th>TAP Transceiver</th>
<th>TAPmax</th>
<th>TIC (slot)</th>
<th>SFX I/O Slots</th>
<th>Parallel I/O</th>
<th>Event I/O</th>
<th>ADC / DAC</th>
<th>Trigger</th>
<th>Aux Relays</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFX-TAP2/4/6 (Desktop)</td>
<td>2/4/6</td>
<td>✓</td>
<td>1</td>
<td>32 bit</td>
<td>3</td>
<td>2</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>SFX-TAP8 (Desktop)</td>
<td>8/7</td>
<td>✓</td>
<td>2/3</td>
<td>32 bit</td>
<td>3</td>
<td>2</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SFX-TAP2/4/6/FXT (Fixture)</td>
<td>2/4/6</td>
<td>✓</td>
<td>1</td>
<td>32 bit</td>
<td>3</td>
<td>2</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SFX-TAP8/FXT (Fixture)</td>
<td>8/7</td>
<td>✓</td>
<td>2/3</td>
<td>32 bit</td>
<td>3</td>
<td>2</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SFX-TAP2C/4C (Compact)</td>
<td>2/4 On-Board</td>
<td>32 bit</td>
<td>3</td>
<td>2</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
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<tr>
<td>SFX-TAP4C/CR (Compact)</td>
<td>4 On-Board</td>
<td>32 bit</td>
<td>3</td>
<td>2</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SCANFLEX® Modules

<table>
<thead>
<tr>
<th>Module</th>
<th>Module Type</th>
<th>Channels</th>
<th>VarioCore®</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFX1000</td>
<td>Prototype Module</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>SFX5296</td>
<td>Digital I/O</td>
<td>96</td>
<td>–</td>
</tr>
<tr>
<td>SFX3550</td>
<td>Differential I/O</td>
<td>50</td>
<td>–</td>
</tr>
<tr>
<td>SFX5704</td>
<td>Mixed signal I/O</td>
<td>2</td>
<td>–</td>
</tr>
<tr>
<td>SFX6216</td>
<td>Analog Input</td>
<td>16</td>
<td>–</td>
</tr>
<tr>
<td>SFX1149.4</td>
<td>Analog Test Bus I/O</td>
<td>2</td>
<td>–</td>
</tr>
</tbody>
</table>

JTAG/Boundary Scan Hardware Accessories

CION™, CION-Modules™

The CION™ chip, a product unique to Göpel electronic, is a dedicated user configurable JTAG/Boundary Scan transceiver device. CION-Modules™, providing I/O capabilities to extend the JTAG/Boundary Scan test coverage, can be built directly into test fixtures.

PXI Modules

The large selection of innovative extension modules for the PXI bus platform includes special JTAG/Boundary Scan Power Supplies and Digital I/O and Mixed-Signal I/O modules for integration into PXI based ATE systems.

JTAG/Boundary Scan Probe

The JTAG/Boundary Scan Probe is a specialised product developed to support the user in debugging tasks.

Fixtures, Board Grabber

To simplify test access to bus interfaces such as CPCI/PCI, PC CARD and PCI, Göpel electronic offers off-the-shelf test fixtures. The Board Grabber provides a universal solution for UUT connection and test point access with an open frame and easily positioned nail probes.
JTAG/Boundary Scan throughout the product life cycle

GÖPEL electronic’s innovative products allow the user to utilise JTAG/Boundary Scan technology in new ways to make it an integral part of the product life cycle, and to apply it in all corporate structures involved in product design, manufacturing and test. SYSTEM CASCON™, designed as a JTAG/Boundary Scan Operating System, acts as the backbone for the setup of a complete test and ISP infrastructure based on access through the Test Access Port defined in IEEE 1149.1. No matter whether individual users work with SYSTEM CASCON™ through a node-lock license, a network license or on integrations in other ATE: project data can easily be transferred worldwide. Together with the intelligent system features, this provides for superior productivity of processes such as rapid design validation and prototype verification, management of design changes or firmware upgrades, rapid New Product Introduction (NPI) in production, or creation of mixed test strategies.

In addition to powerful stand-alone test setups, GÖPEL electronic also offers complete test systems with integrated JTAG/Boundary Scan. The SCANTURY® BScan Prober, SCANTURY® PXI 50xx Series Tester and the OptiCon AOI system family are examples. Complete integration packages are available for all leading Flying Probe Testers and In-Circuit-Testers.
The people at TietoEnator share this opinion. They are excited by the extraordinary good support. But that’s not all. TietoEnator produces PCBs with very high packing density, double sided packed BGAs and more than 2,000 nets. Traditional test strategies were not able to achieve the necessary test depth anymore because of the lack of test points and the available space. JTAG/Boundary Scan was discovered as a reliable test technology. After comparing various suppliers the following were decisive in choosing GÖPEL electronic:

• hardware engineering
• the software development plans
• the high level of support
• the range of functions and simple user interface

Besides testing of prototypes already at the very beginning. Time is highly important. Between the device’s development and the series production 2-3 test runs are made. Without using JTAG/Boundary Scan two additional stages would be required which would mean a delay of 4-6 weeks. JTAG/Boundary Scan is universally used as part of the board test, and for the programming of EEPROMs, CPLDs and Flashes, and verification of components.

GOPEL electronic which, in particular, is beneficial for mixed technology PCBs. JTAG/Boundary Scan filled the test gap, the ICT leaves, without problems. “Since the trend is moving to ever more complex components, JTAG/Boundary Scan is irreplaceable,” say the test engineers. “Focussing on it was the right decision.”

The decision for SYSTEM CASCON™ from GÖPEL electronic was made because of the software structure and the well organized interface.

JTAG/Boundary Scan - a comprehensively applied and accepted standard

Many international companies have fully embraced the benefits of JTAG/Boundary Scan. They know that a thorough test strategy is needed to determine the correctness of electronic assemblies. JTAG/Boundary Scan is able to test highly complex boards and guarantees the required test depth. Lucent Technologies uses JTAG/Boundary Scan in the development of PCBs. Before the production stage, the boards must go through various development stages and are tested via JTAG/Boundary Scan several times. Changes necessary to improve coverage will be made at the design stage. JTAG/Boundary Scan is an integral part of the product philosophy from the very beginning. Time is highly important. Between the device’s development and the series production 2-3 test runs are made. Without using JTAG/Boundary Scan two additional stages would be required which would mean a delay of 4-6 weeks. JTAG/Boundary Scan is universally used as part of the board test, and for the programming of EEPROMs, CPLDs and Flashes, and verification of components.

Without BScan there would be a growing test gap in respect of highly complex components such as BGAs and µBGAs. Lucent Technologies decided in favour of JTAG/Boundary Scan from GÖPEL electronic because they are convinced by the product’s quality, a “quality other vendors do not supply.”

Siemens Transportation Systems uses JTAG/Boundary Scan at the production stage, where products with a very long life cycle are manufactured. They rely on standards which guarantee the future of the test method. In 1997, the Siemens engineers learned about JTAG/Boundary Scan. Safety-relevant boards were not completely accessible with test points for the In-Circuit structural test with a nail bed adapter. JTAG/Boundary Scan solved the problem. Today, the method is seen as a technical necessity. Devices, which cannot be tested by ICT, are tested with JTAG/Boundary Scan from GÖPEL electronic which, in particular, is beneficial for mixed technology PCBs. JTAG/Boundary Scan filled the test gap, the ICT leaves, without problems. “Since the trend is moving to ever more complex components, JTAG/Boundary Scan is irreplaceable,” say the test engineers. “Focussing on it was the right decision.”

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The people at TietoEnator share this opinion. They are excited by the extraordinary good support. But that’s not all. TietoEnator produces PCBs with very high packing density, double sided packed BGAs and more than 2,000 nets. Traditional test strategies were not able to achieve the necessary test depth anymore because of the lack of test points and the available space. JTAG/Boundary Scan was discovered as a reliable test technology. After comparing various suppliers the following were decisive in choosing GÖPEL electronic:

• hardware engineering
• the software development plans
• the high level of support
• the range of functions and simple user interface

Besides testing of prototypes already at the development stage, TietoEnator uses JTAG/Boundary Scan in the entire life cycle of their products – for testing and programming. The use of JTAG/Boundary Scan is especially beneficial in the case of re-designs, because an ICT would require a completely new bed of nails which would mean the loss of time and money.

“From the beginning we were very satisfied. The system has worked reliably. The service and the extended hardware and software are unbeatable,” say the test engineers.
GÖPEL electronic and our partners guarantee you extended technical support. As the world-leading provider of intelligent tools for extended Boundary Scan, we have been customer driven since the company's foundation in 1991. Together with our reliable distribution and support centres, we supply excellent products combined with comprehensive after-sales service and support. This way the vast experience gained from more than 70,000 successful test projects is turned into your individual benefit.

Comprehensive support & service for Your success
As with all new technologies, Boundary Scan is very support intensive in the introductory phase, and we still encounter new possibilities of this exciting approach.

Further information
Please feel free to order the interactive teaching software Boundary Scan Coach directly from us, or download it from our website www.goepel.com

Worldwide support for our global customer base
- GÖPEL electronic corporate offices
- Authorized distributors/VARs
- Authorized support centers

Comprehensive support throughout the entire product life cycle
- Seminars for basic and advanced Boundary Scan (2 day classes)
- In-house seminars with individual agendas
- Hands-on system training (2 day class) as training on the job
- Worldwide Boundary Scan Days® (meetings for users and interested parties)

Through GÖPEL electronic's special support website GENESIS our customers have access to a wide variety of information and data including the latest component libraries, software updates, user manuals and application notes.